

Compal Confidential

PBJ20 Schematics Document

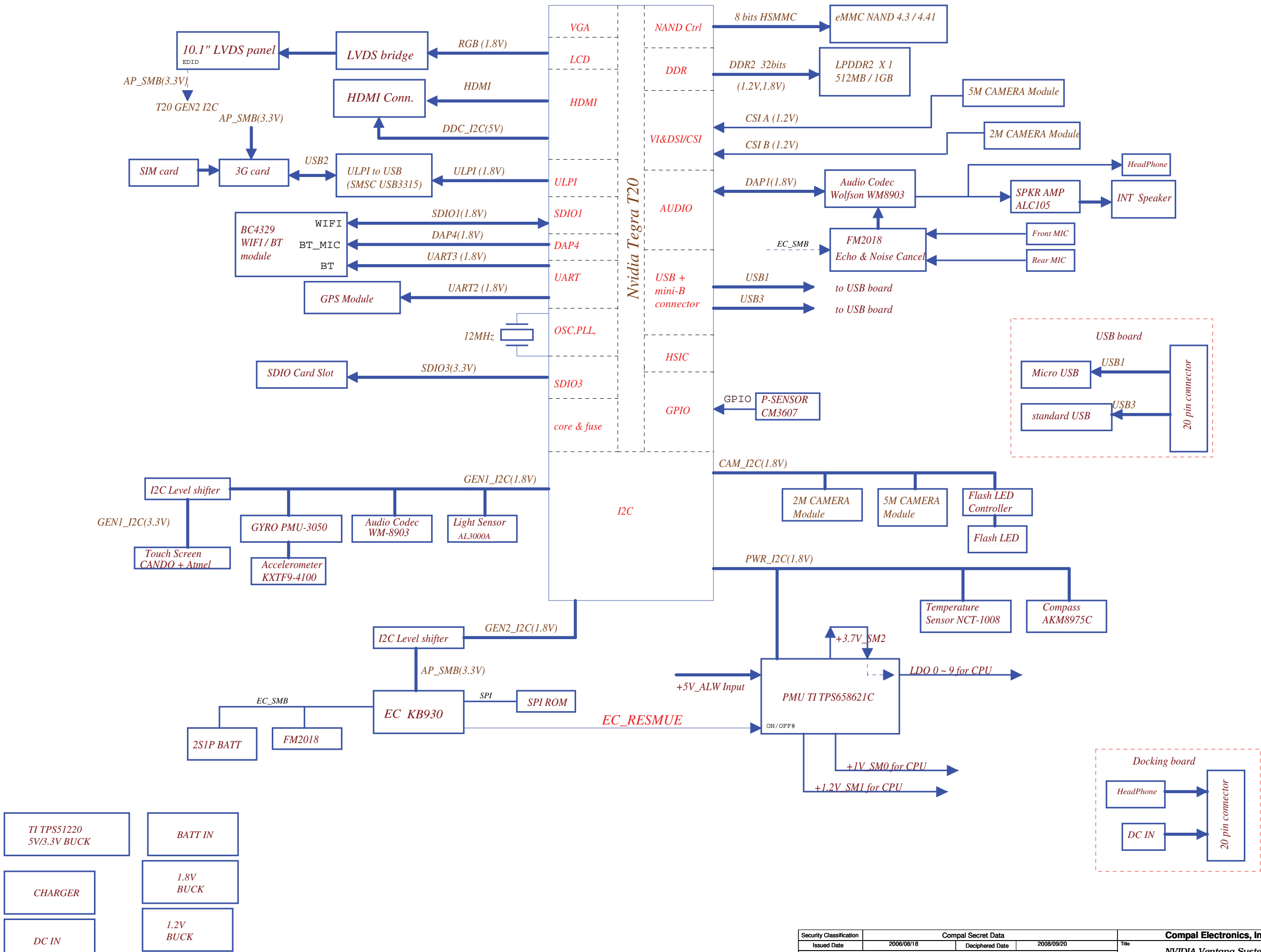
Nvdia(T20) + LPDDRII

2010-10-07

REV: 0.4

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PBJ20 system block diagram



Voltage Rails

Power Plane	Description	IDLE	Standby
VIN	Adapter power supply (12V)	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON
+1.2VS_SM0	Core voltage for CPU	ON	ON
+1.0VS_SM1	CPU voltage for CPU	ON	OFF
+1.1VS_LDO1	AVDD_PLL power rail	ON	OFF
+1.2VS_LDO2	T20 RTC power rail	ON	OFF
+1.8VS_LDO4	T20 system power rail	ON	ON
+3.3VS_LDO3	T20 USB power rail	ON	OFF
+2.85VS_LDO5	Core voltage for EMMC	ON	OFF
+2.85VS_LDO6	Core voltage for CAMERA	ON	OFF
+3.3VS_LDO7	T20 HDMI power rail	ON	OFF
+1.8VS_LDO8	T20 HDMI PLL power rail	ON	OFF
+2.85VS_LDO9	T20 DDR RX power rail	ON	ON
+3VALW	3.3V always on power rail	ON	ON
+3VS	3.3V switched power rail for standby mode	ON	OFF
+5VALW	5V always on power rail	ON	ON
+1.8V	1.8V always on power rail	ON	ON
+1.8VS	1.8V switched power rail for standby mode	ON	OFF
+3.3VS_RTC	RTC power	ON	ON

STATE \ SIGNAL	EC_SYS_STANDBY#	EN_VDD_+1.8VS_S3	EN_VDD_3V3	EN_VDD_1V8
Full ON	High	High	High	High
Standby	High	High	High	High

PWR_I2C address

Device	Address
PMU	0110 100X b
E-Compass	
Temperature sensor	1001 100X b

CAM_I2C address

Device	Address
CAMERA 5M	0110 110X b
CAMERA 1.3M	1001 000X b
LED FLASH	

GEN1_I2C

Device	Address
Audio Codec	1001 010xb
Light sensor	0100 010xb
Gyro	1101 000xb

TS_I2C

Device	Address
Touch Panel	0100 110xb

GEN2_I2C

Device	Address
--------	---------

AP_SMB

Device	Address
PANEL EDID	
3G Card	
EC	

EC_SMB

Device	Address
Echo Cancellation	1011 111xb
BATT	

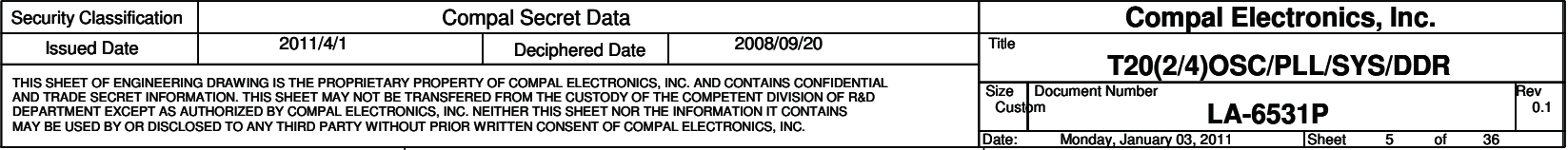
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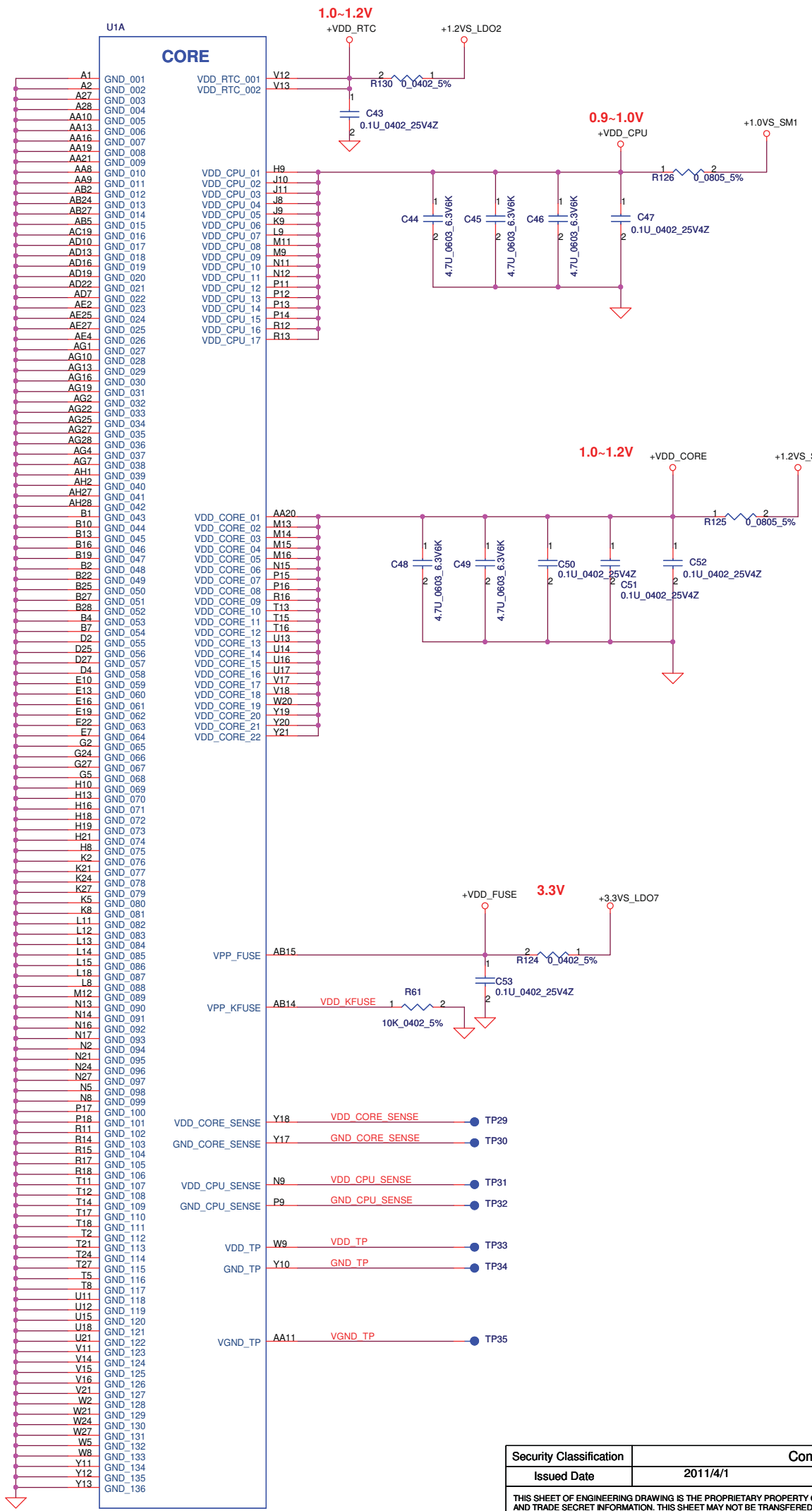
Device	Address
G-sensor	0000 1111 b

DDC_I2C

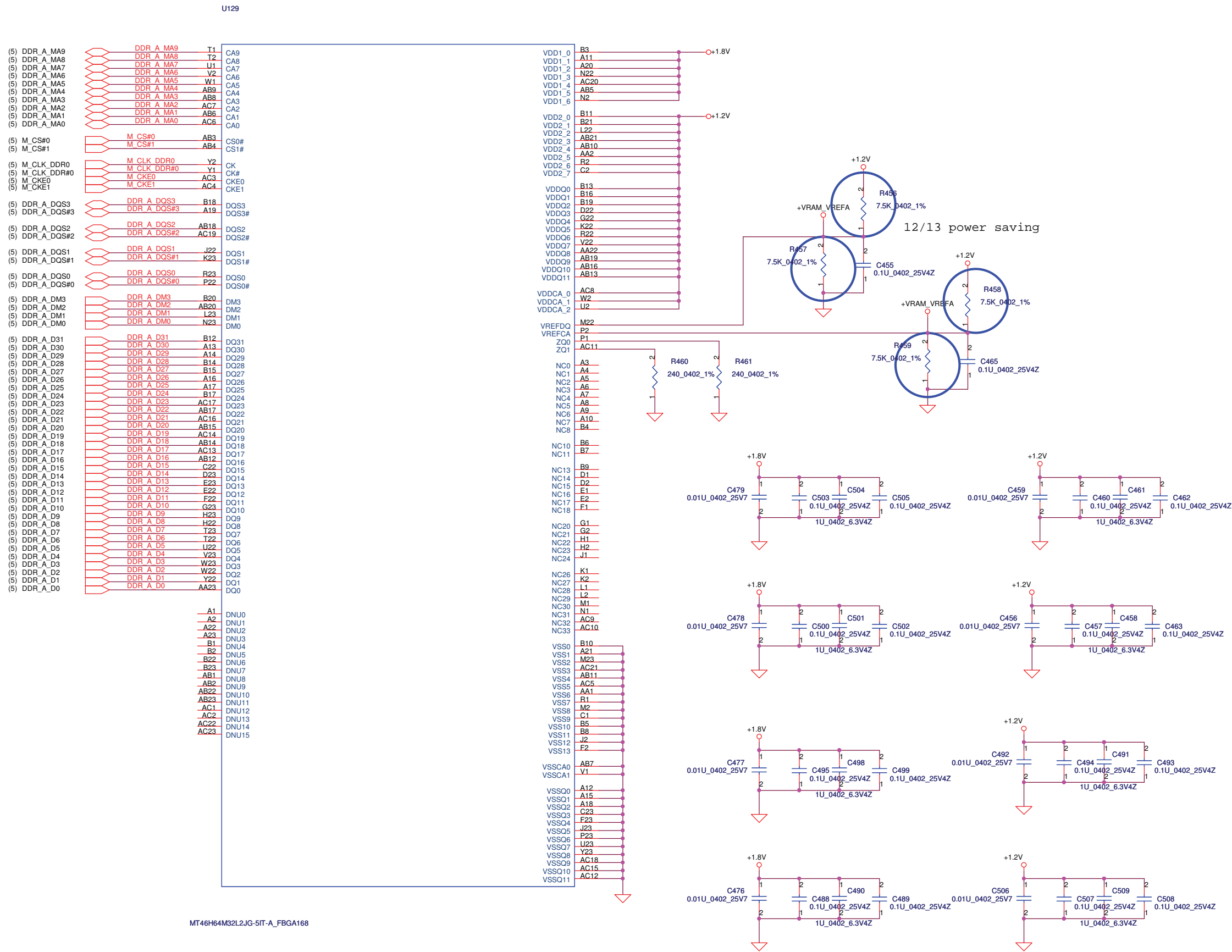
Device	Address
HDMI EDID	1010 000xb

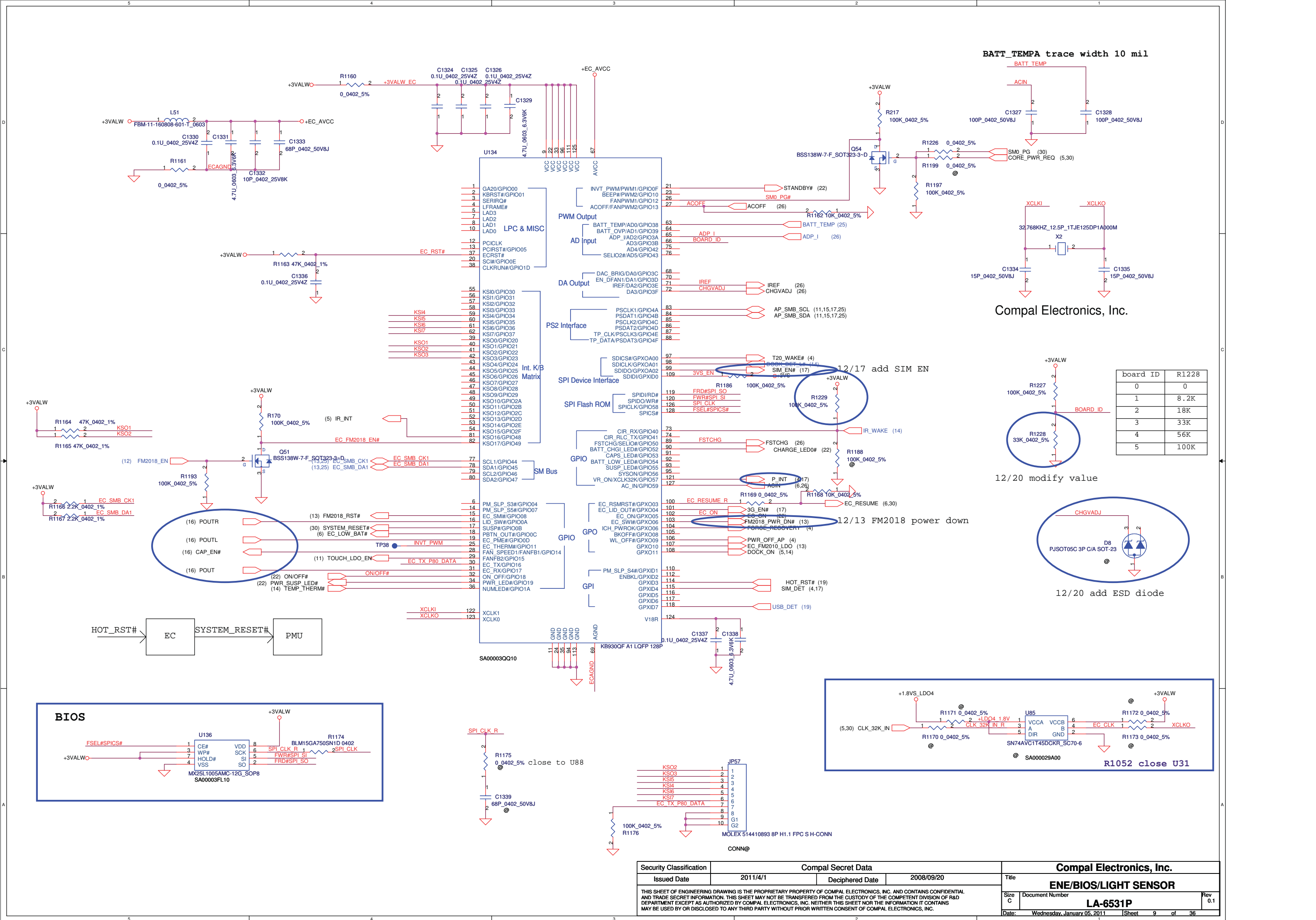


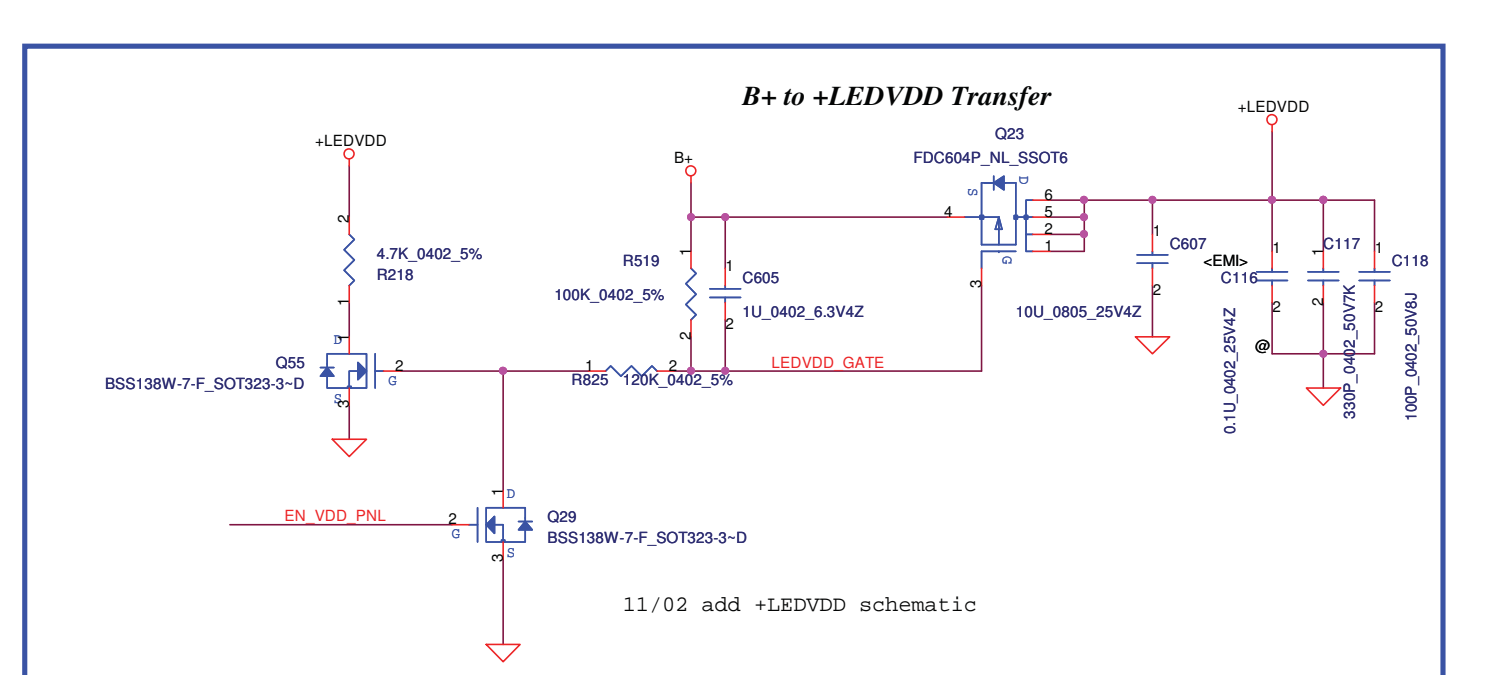
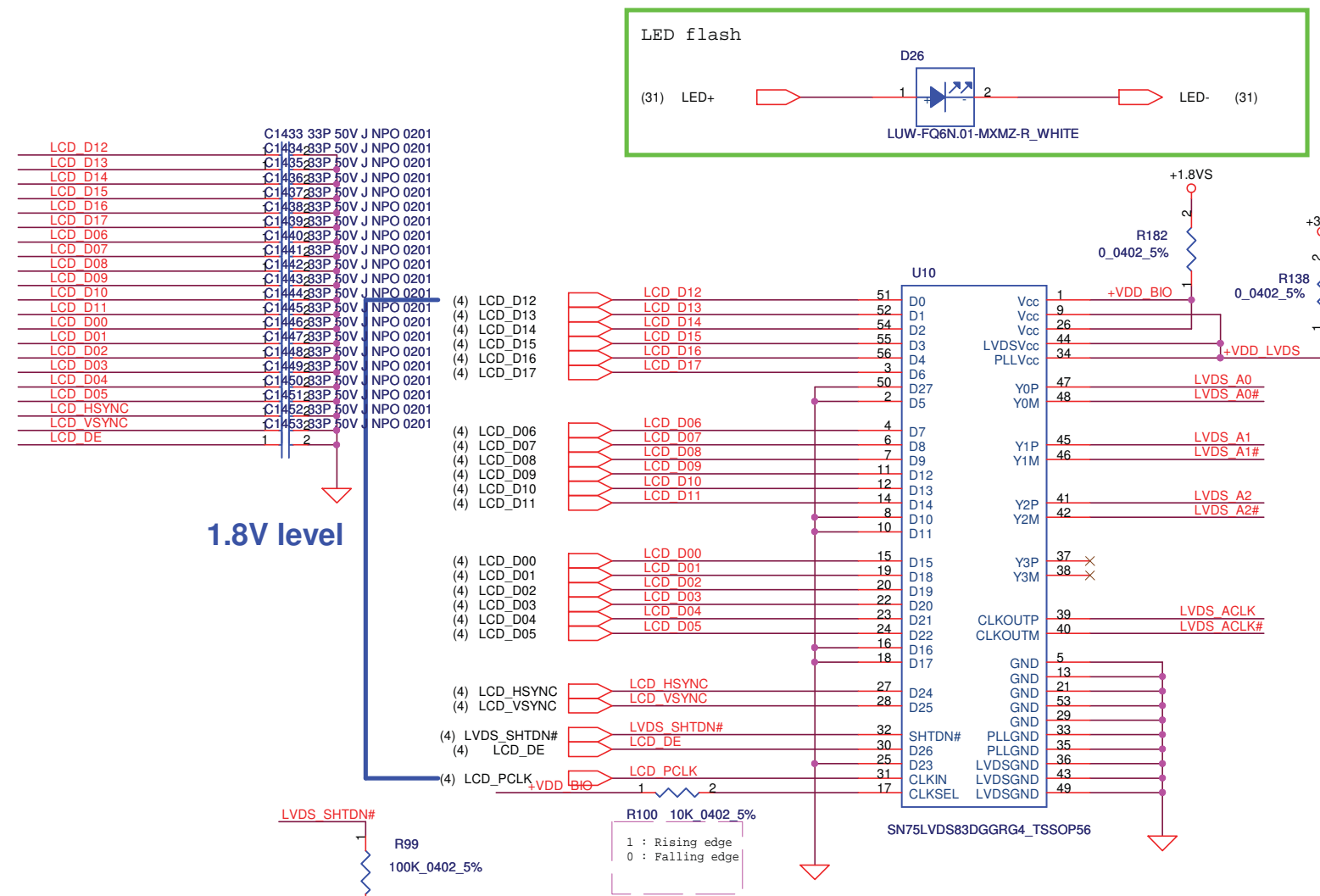




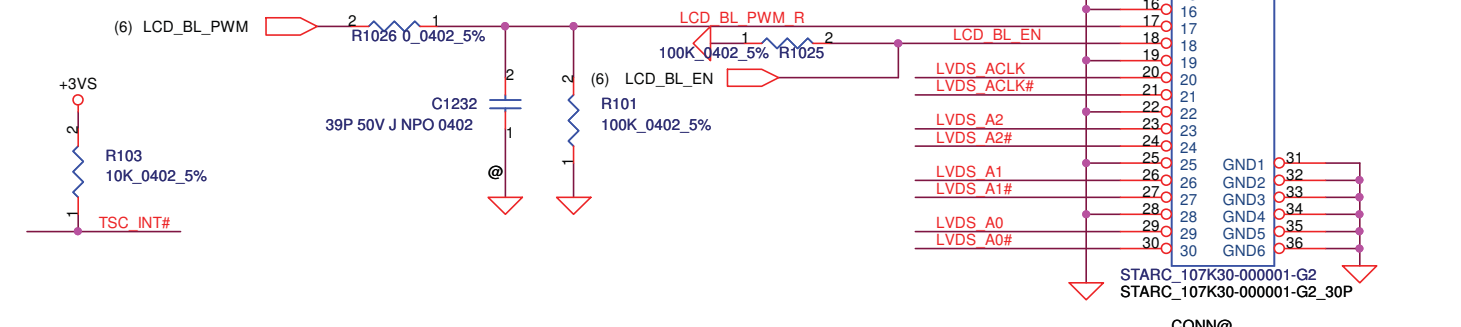
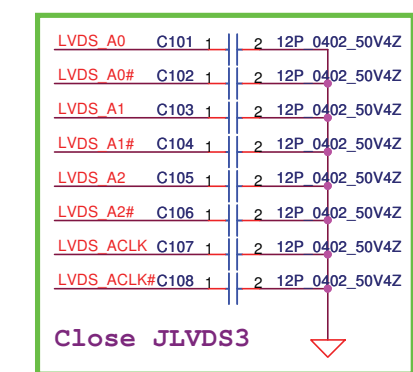
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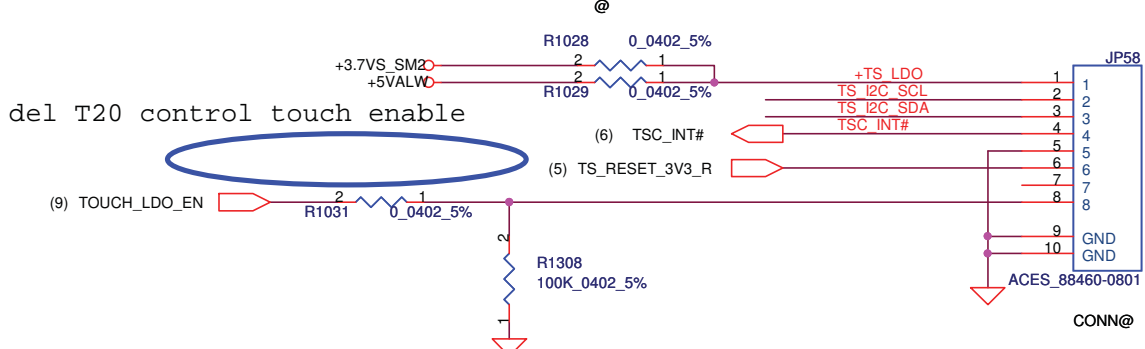




+LEDVDD circuit

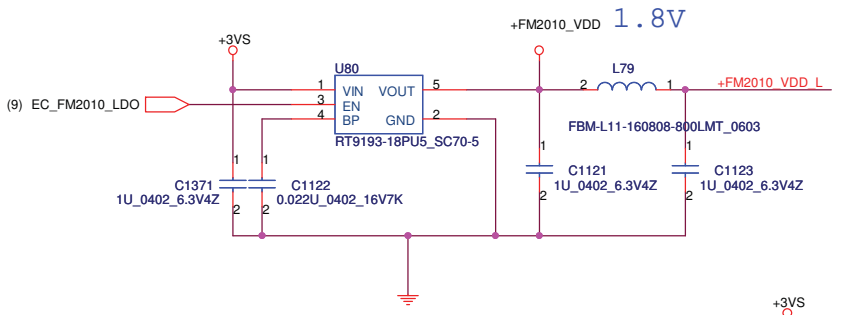


12/16 del T20 control touch enable

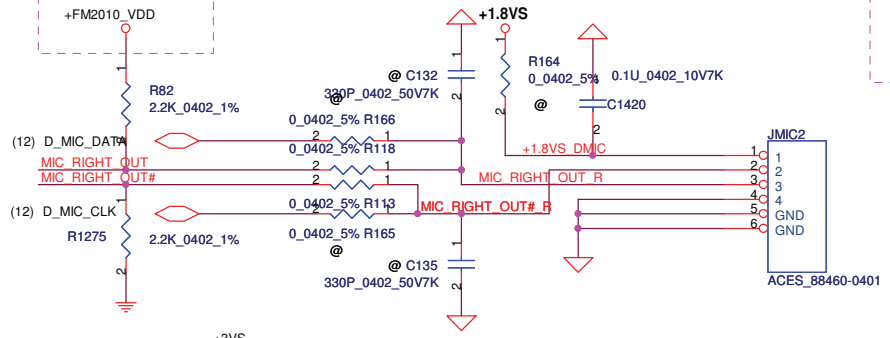


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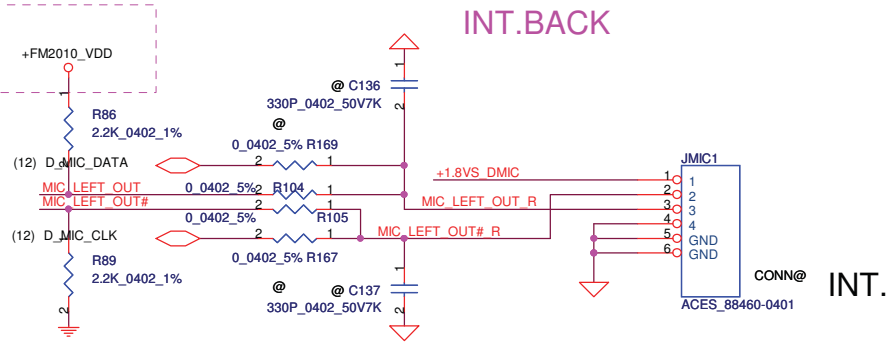




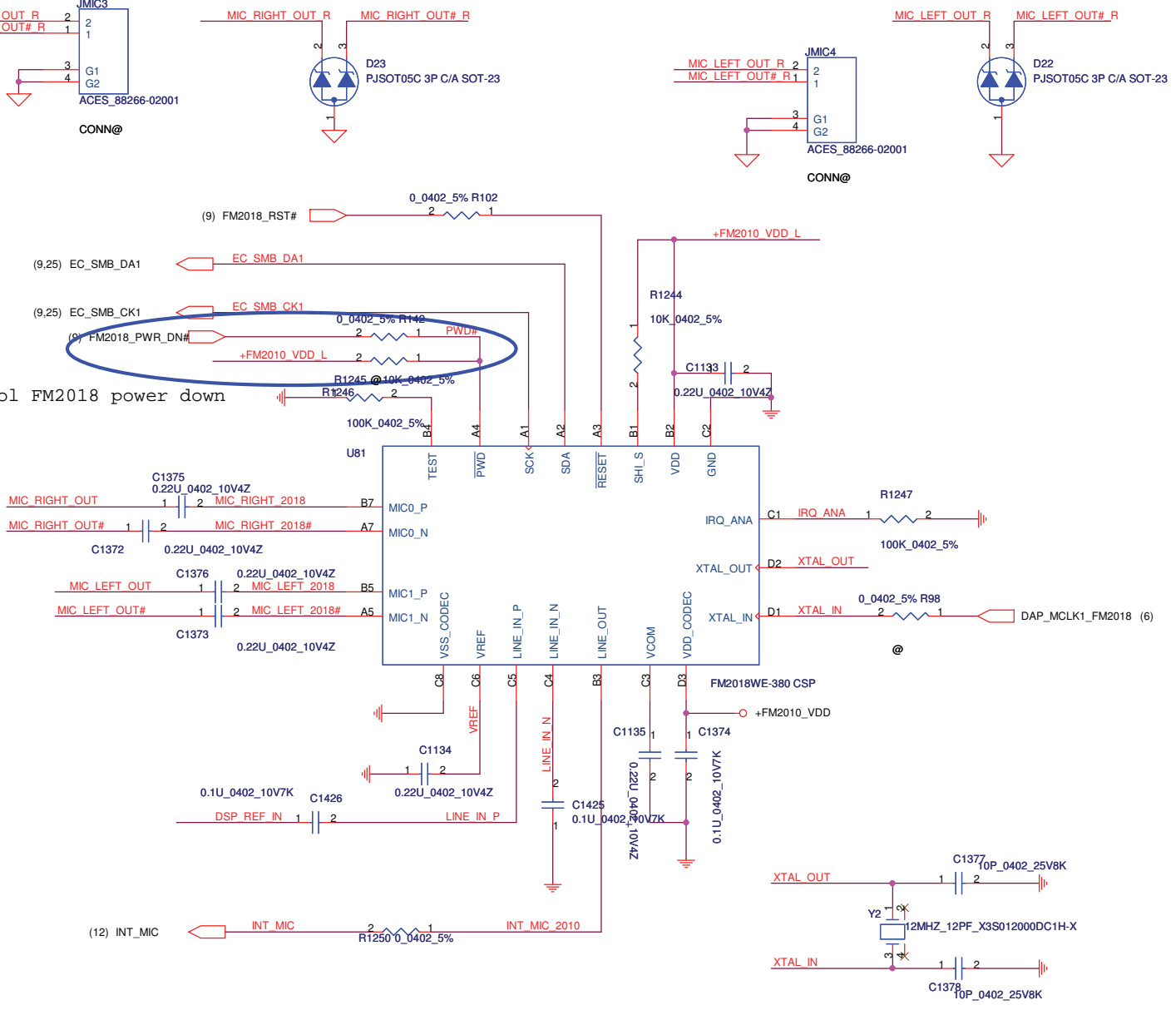
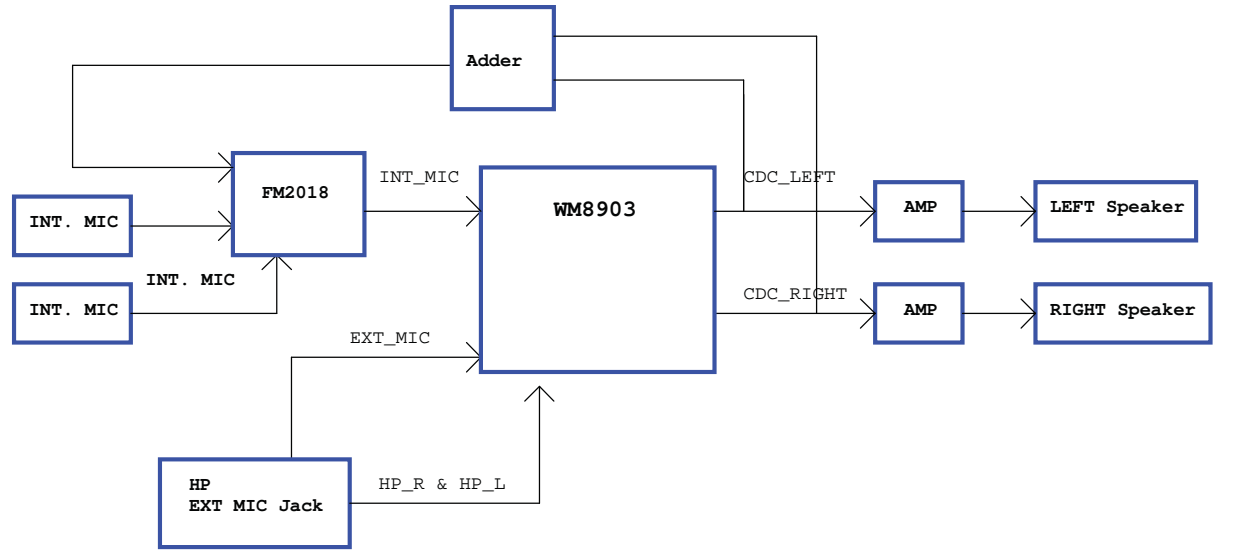
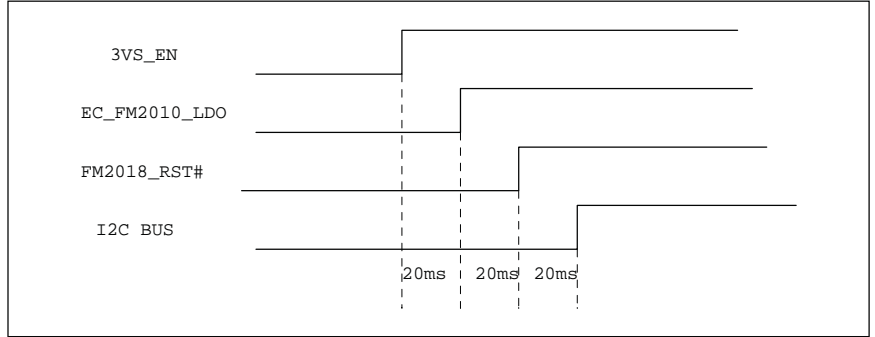
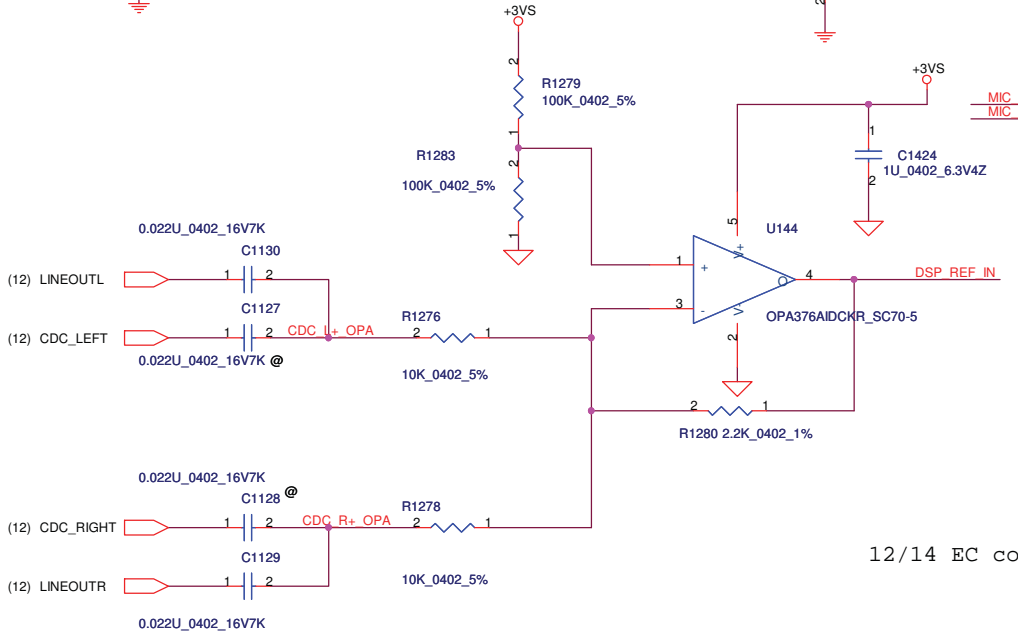
INT. FRONT



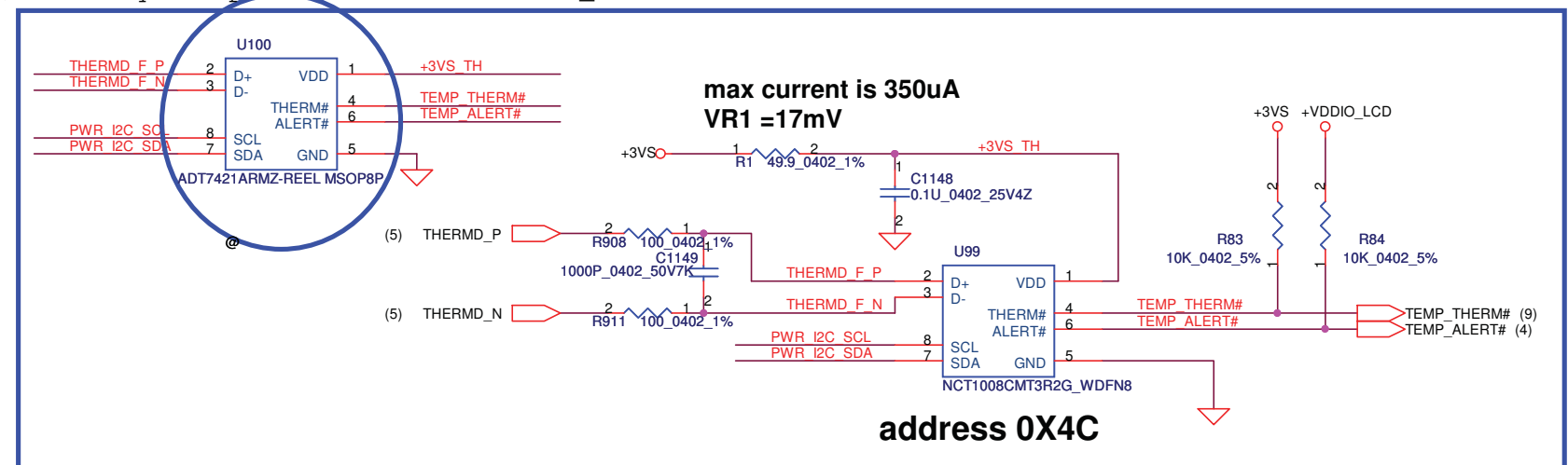
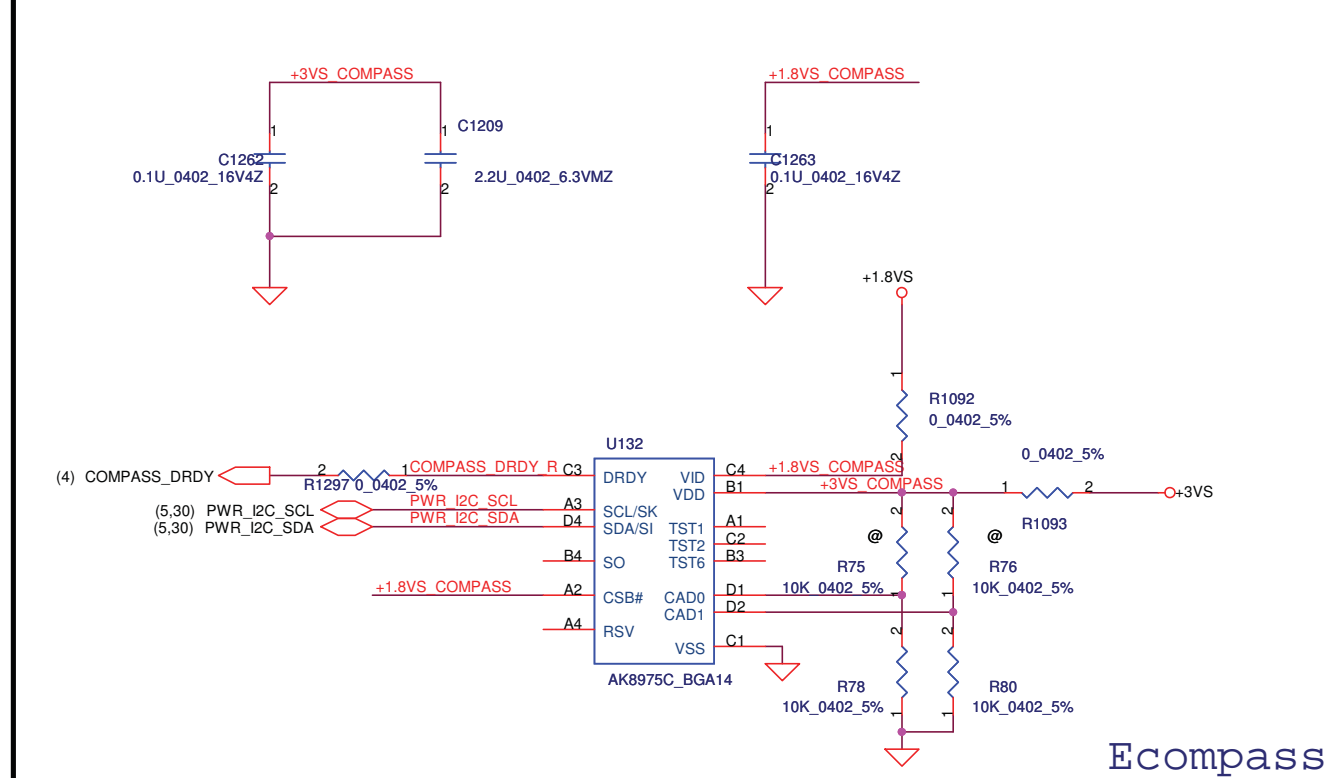
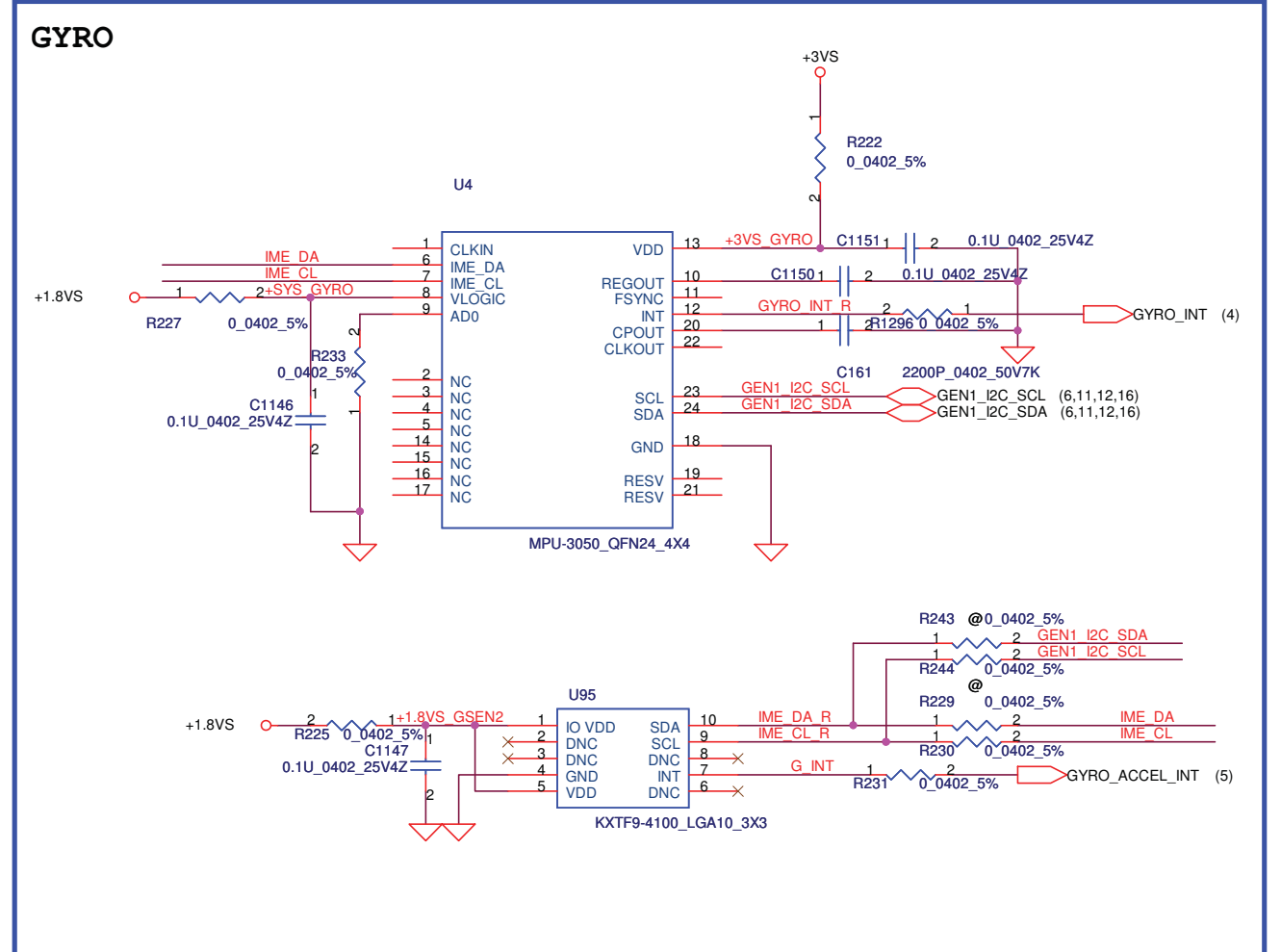
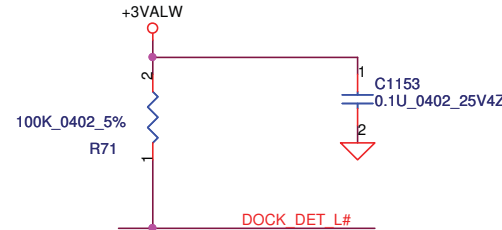
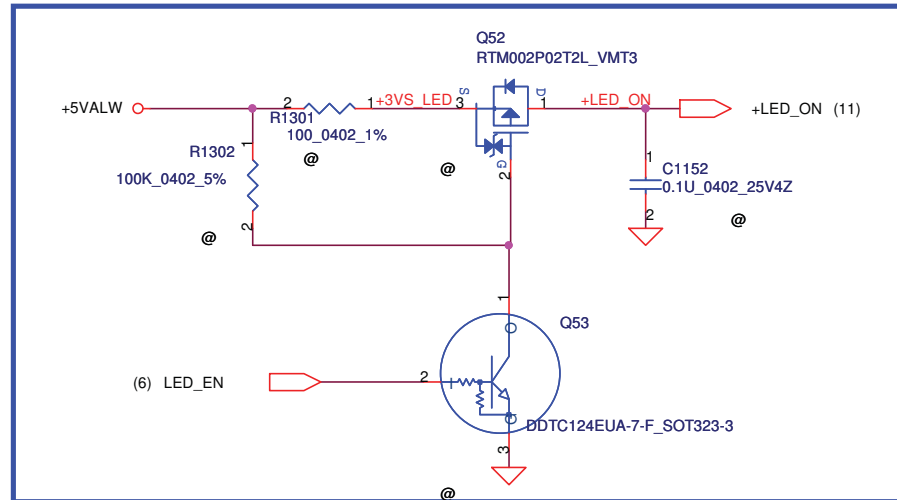
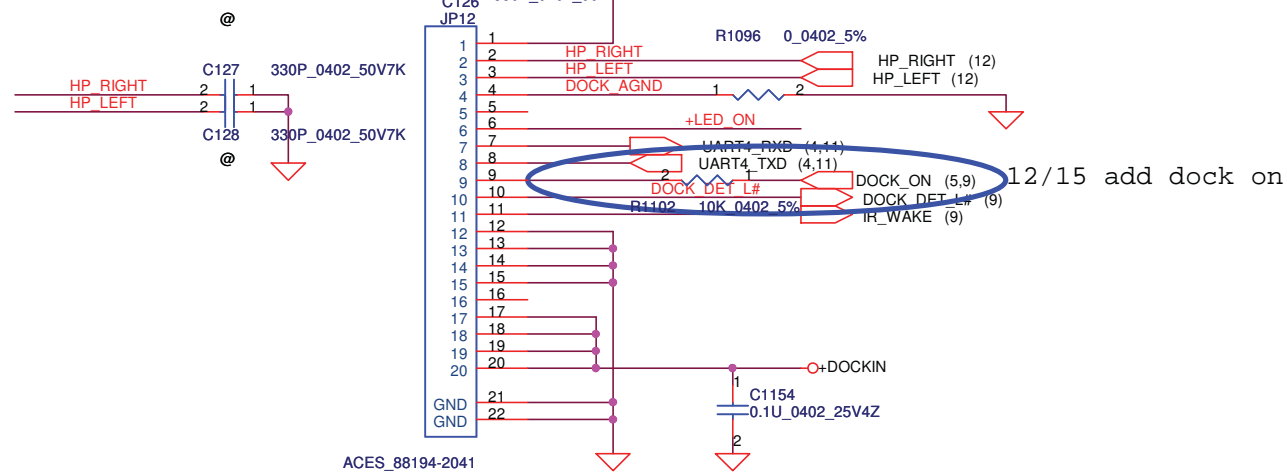
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INT. MIC



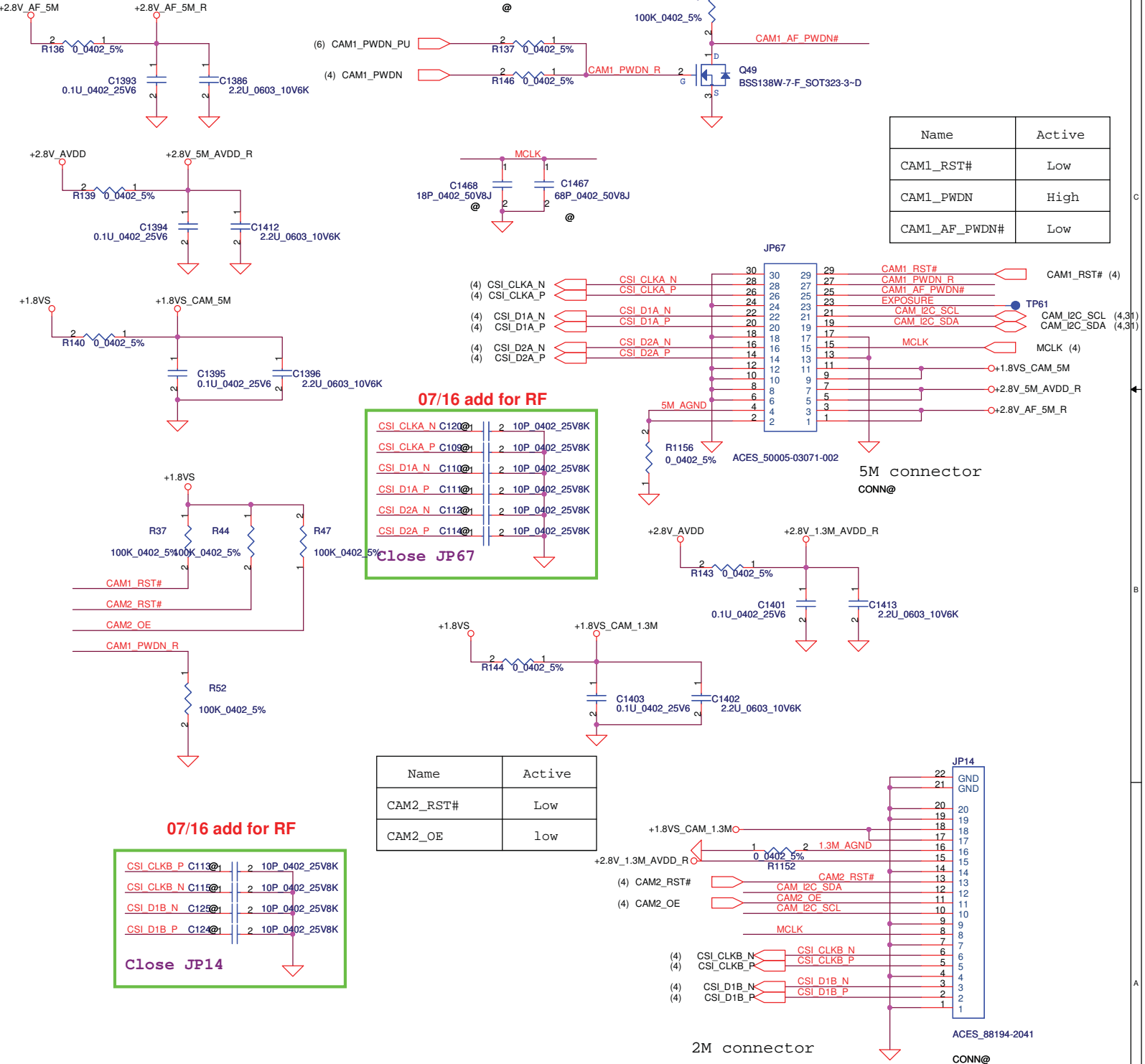
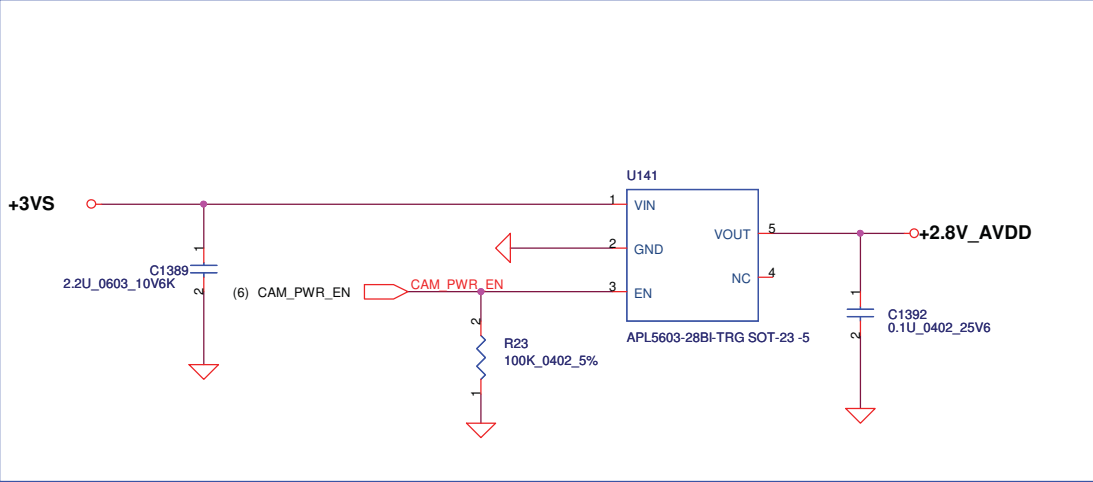
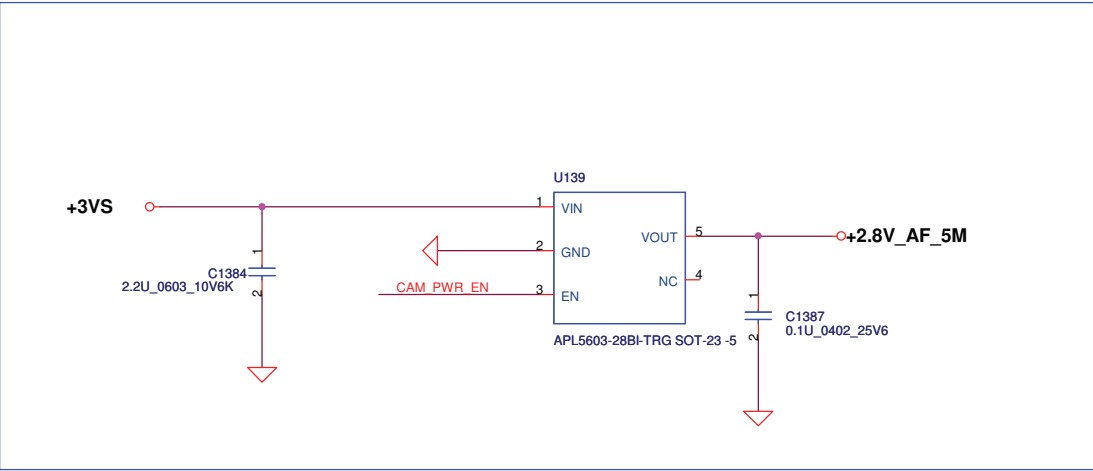
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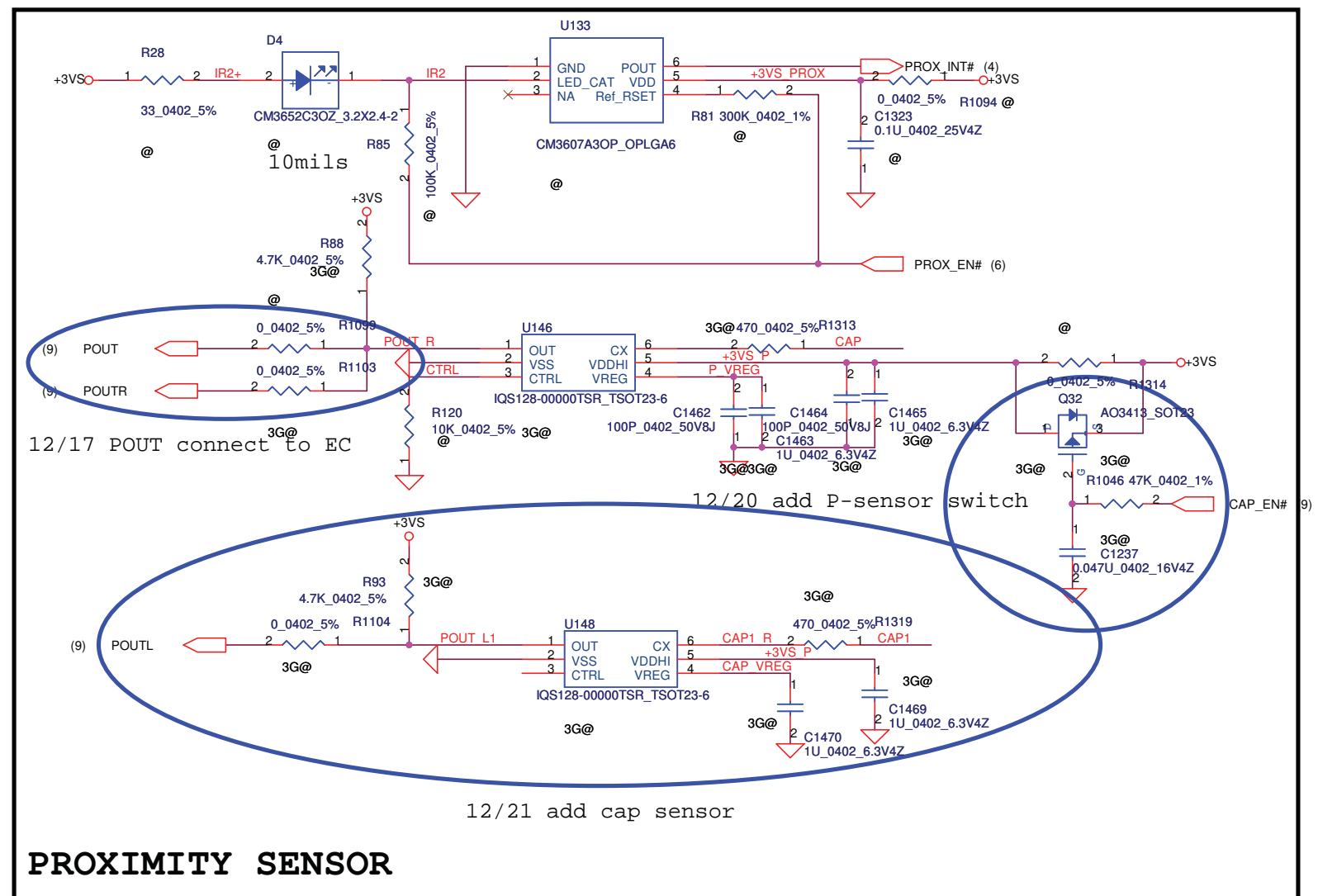
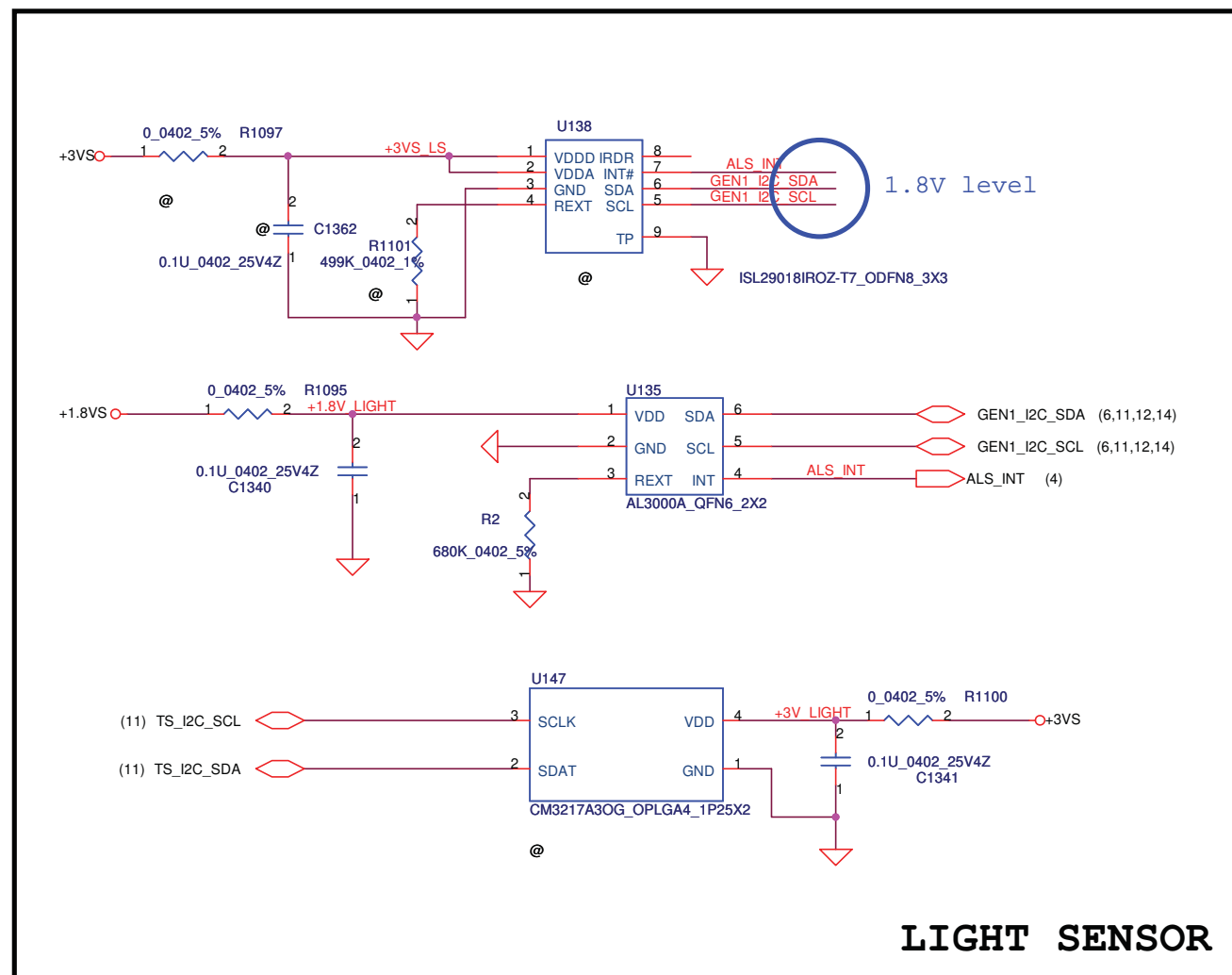
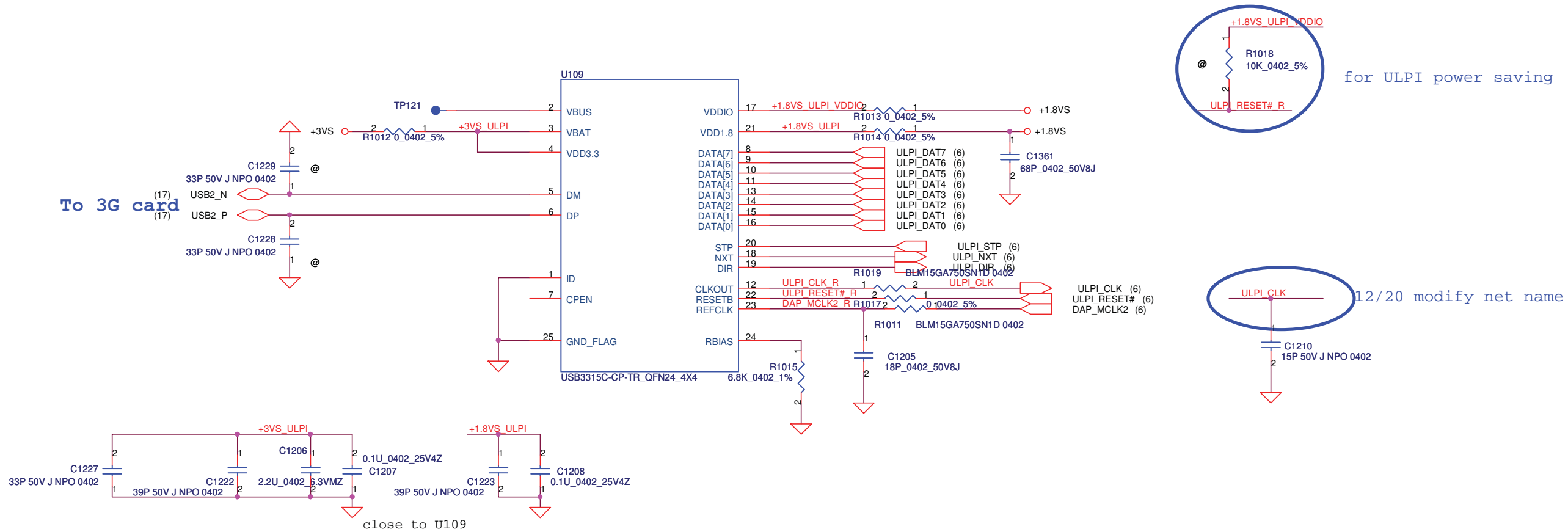
Level shift

The schematic diagram illustrates a level shifter circuit for the PCA9306DCUR_VSSOP8. The circuit is designed to interface between a 1.8V level and a 3.3V level. The 1.8V side includes a 2.2K_0402_1% resistor (R153), a 2.2K_0402_1% resistor (R154), and a 0.1U_0402_25V4Z capacitor (C209). The 3.3V side includes a 200K_0402_1% resistor (R958), a 0.1U_0402_25V4Z capacitor (C210), a 2.2K_0402_1% resistor (R156), and a 2.2K_0402_1% resistor (R236). The level shifter is connected to the GEN2_I2C_SCL and GEN2_I2C_SDA lines on the 1.8V side and the AP_SMB_SCL and AP_SMB_SDA lines on the 3.3V side.

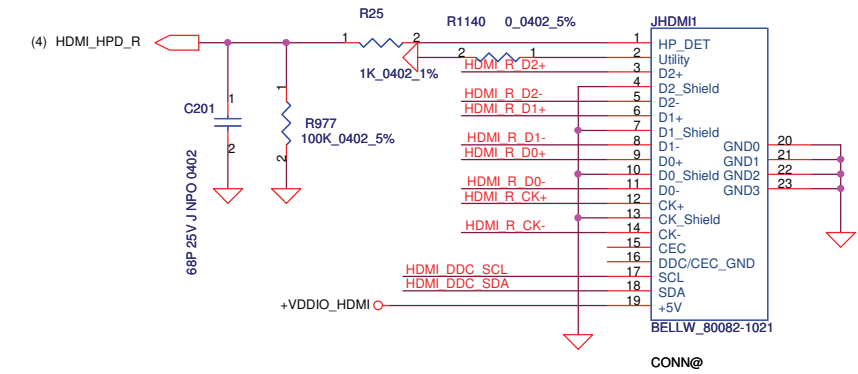


Name	Active
CAM2_RST#	Low
CAM2_OE	low

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[illegible]

(4) HDMI_TXCP HDMI_TXCP

1 R188 2
@ 0_0402_5%

4 3

5 L12 3

1 2

WCM-2012HS-900T_0805

(4) HDMI_TXCN HDMI_TXCN

1 R171 2
@ 0_0402_5%

4 3

5 L12 3

1 2

WCM-2012HS-900T_0805

(4) HDMI_TXD0P HDMI_TXD0P

1 R172 2
@ 0_0402_5%

4 3

5 L13 3

1 2

WCM-2012HS-900T_0805

(4) HDMI_TXD0N HDMI_TXD0N

1 R173 2
@ 0_0402_5%

4 3

5 L13 3

1 2

WCM-2012HS-900T_0805

(4) HDMI_TXD1P HDMI_TXD1P

1 R174 2
@ 0_0402_5%

4 3

5 L14 3

1 2

WCM-2012HS-900T_0805

(4) HDMI_TXD1N HDMI_TXD1N

1 R175 2
@ 0_0402_5%

4 3

5 L14 3

1 2

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(4) HDMI_TXD2P HDMI_TXD2P

1 R176 2
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4 3

5 L15 3

1 2

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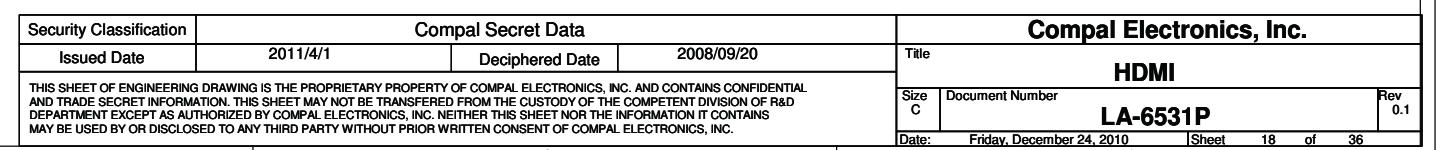
1 R177 2
@ 0_0402_5%

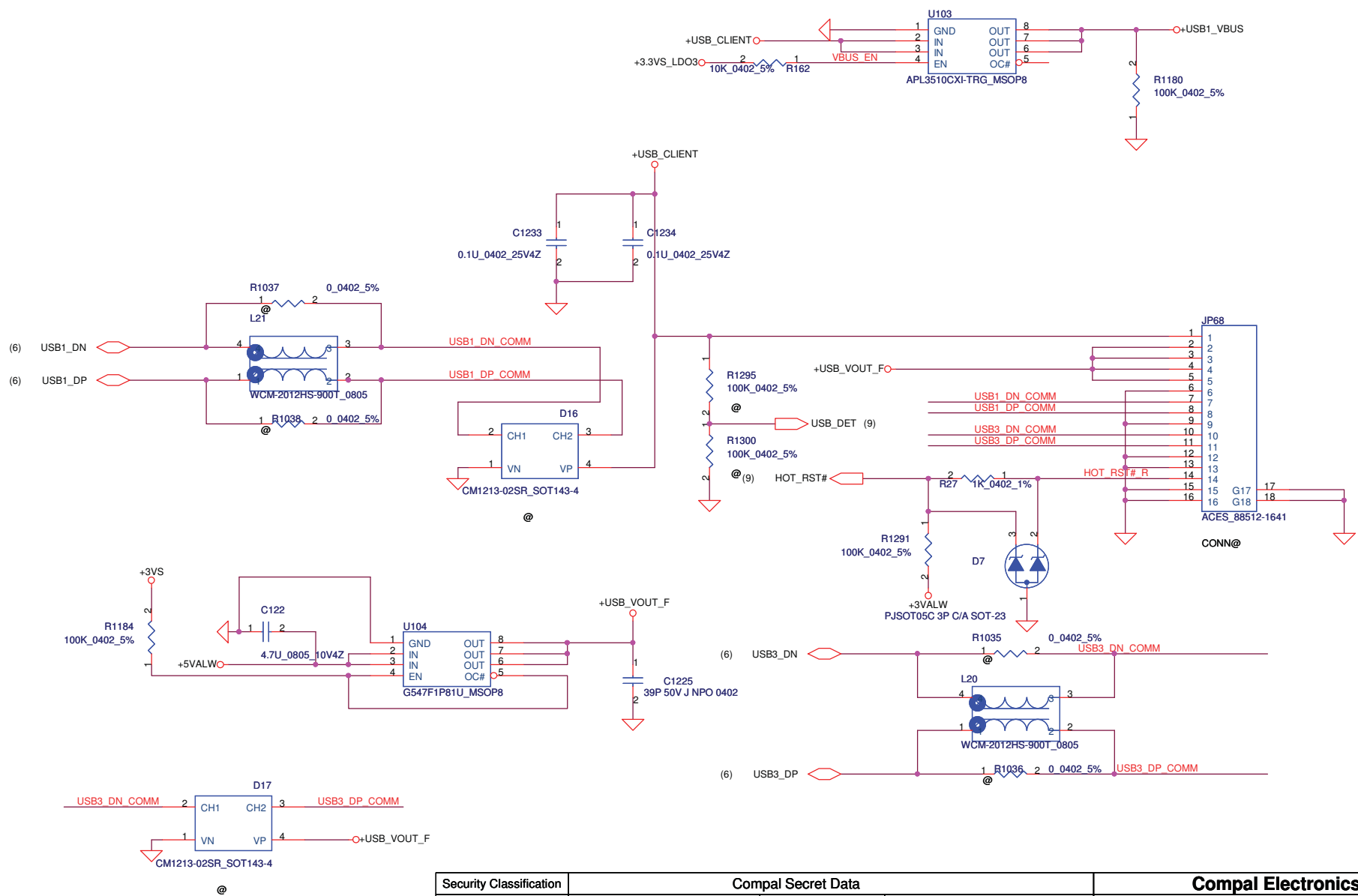
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5 L15 3

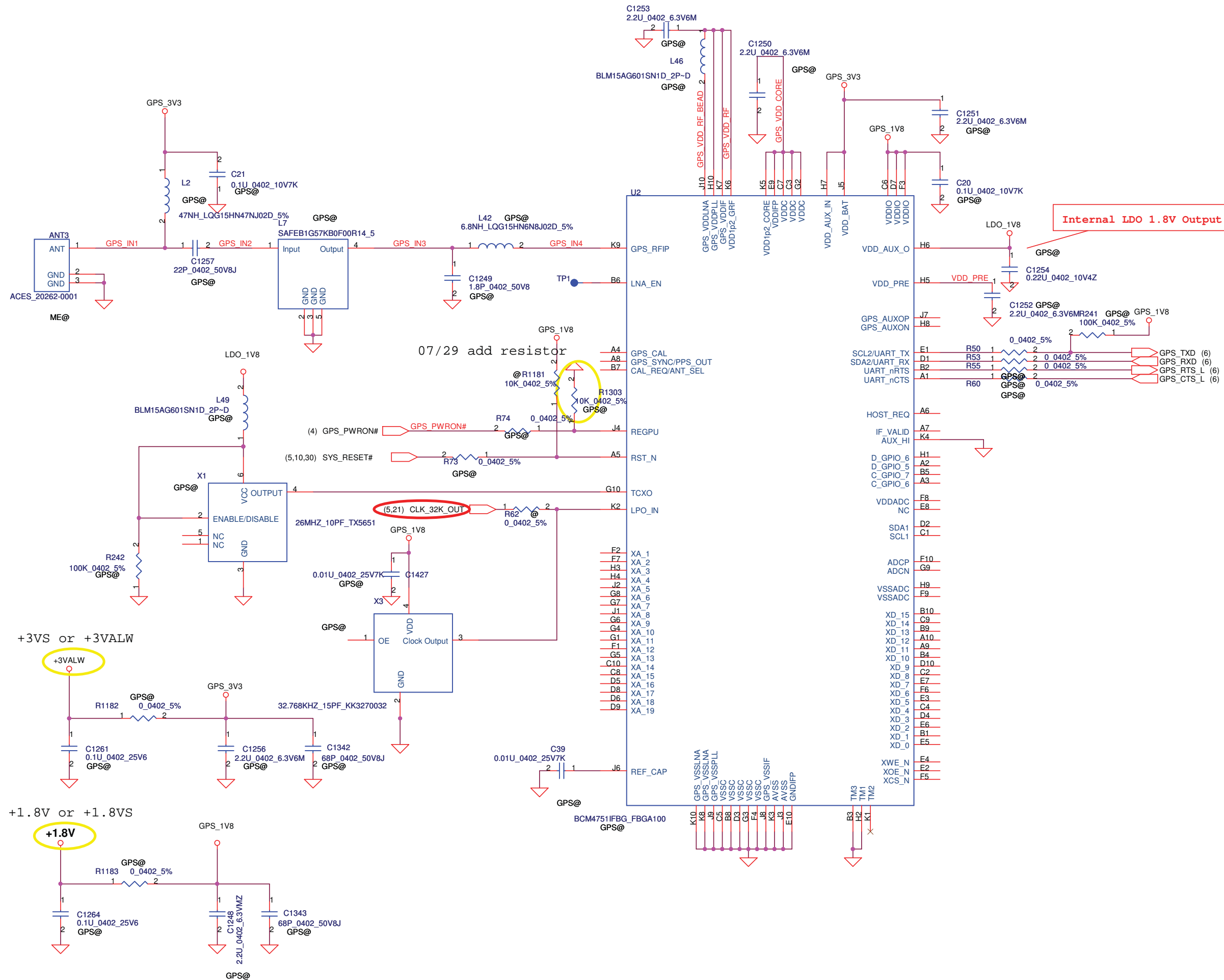
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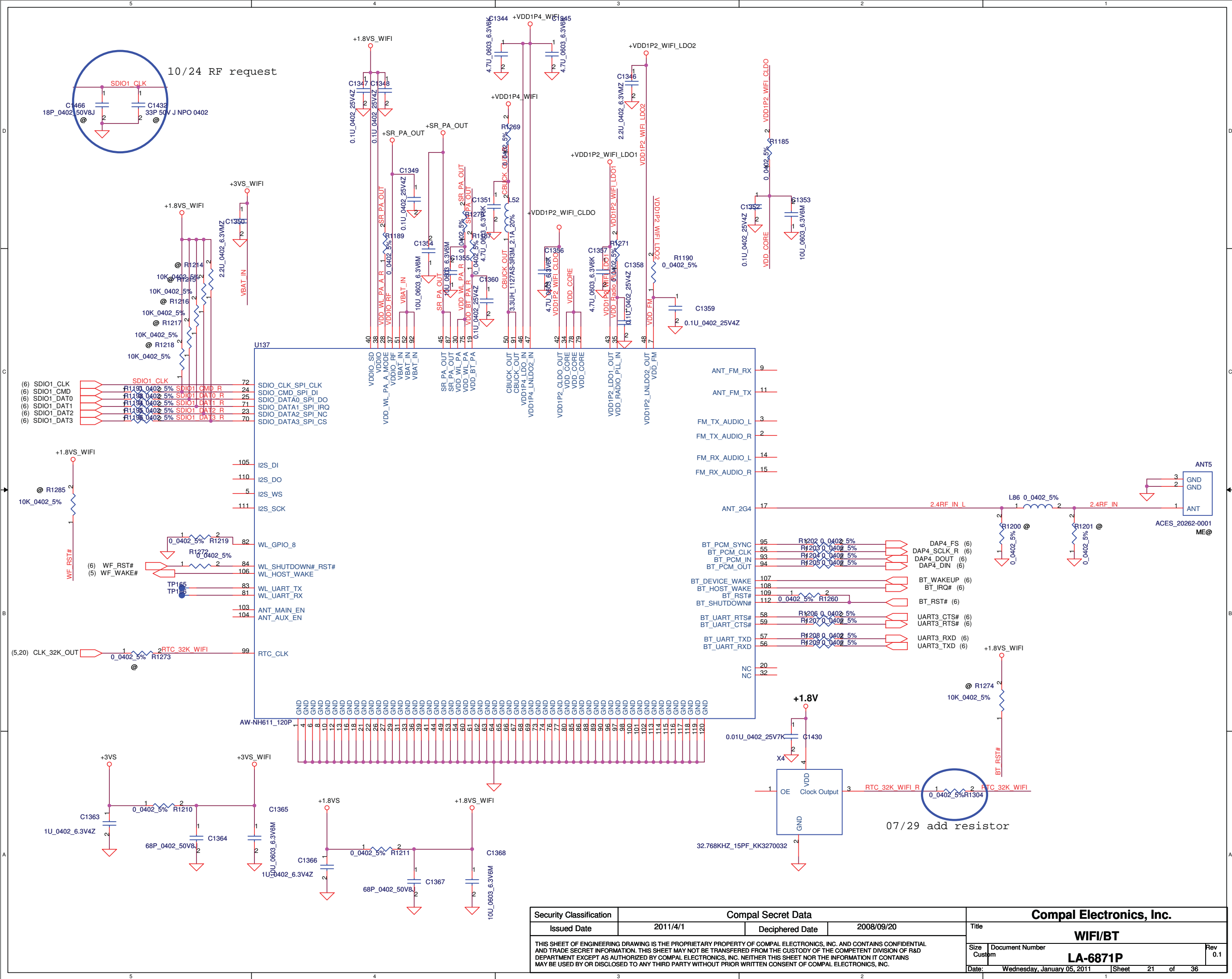




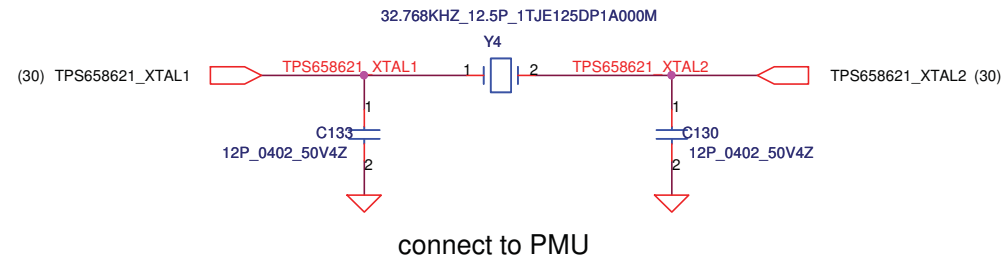
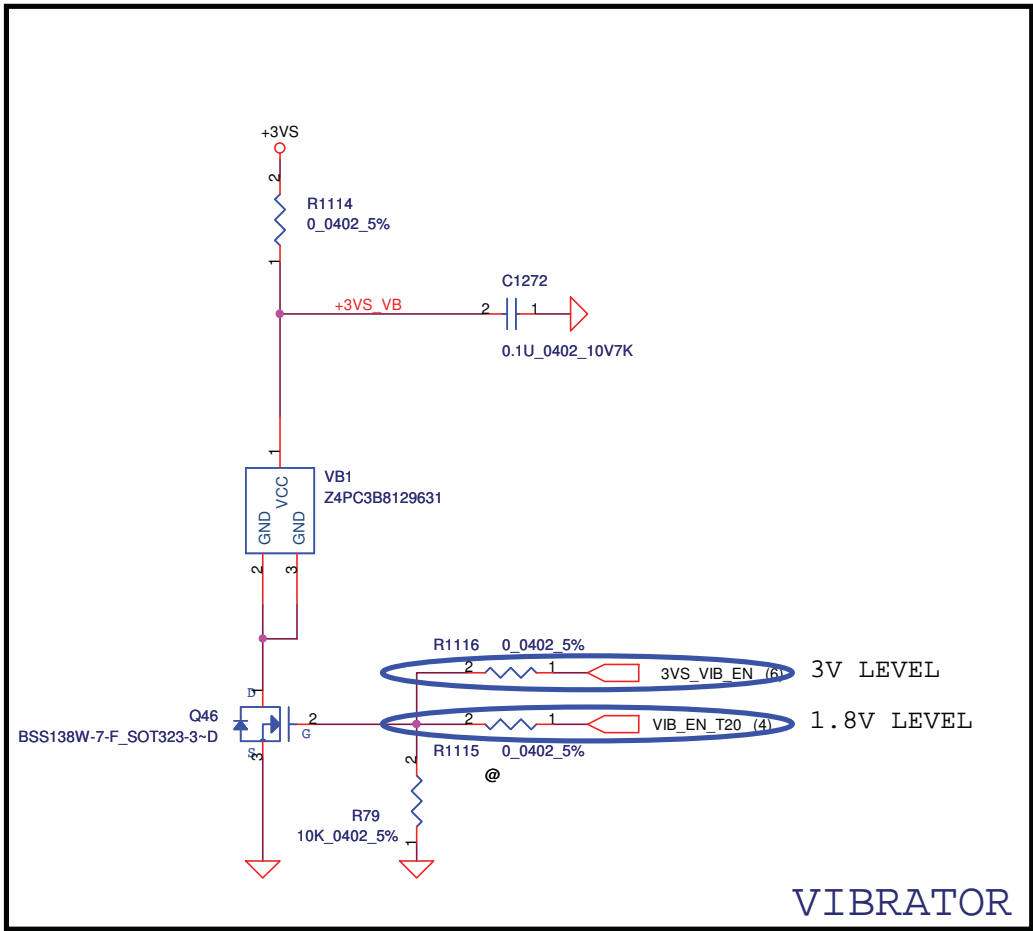
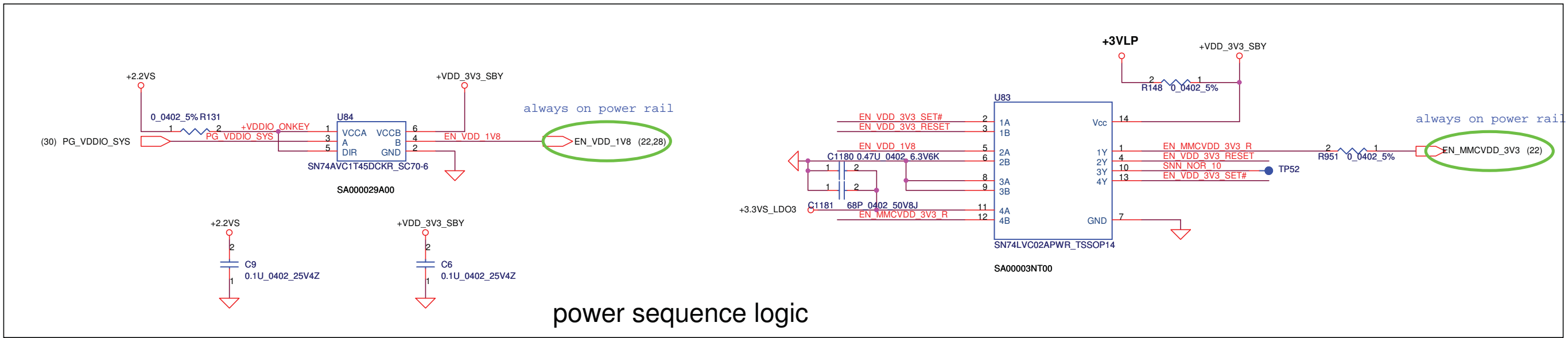
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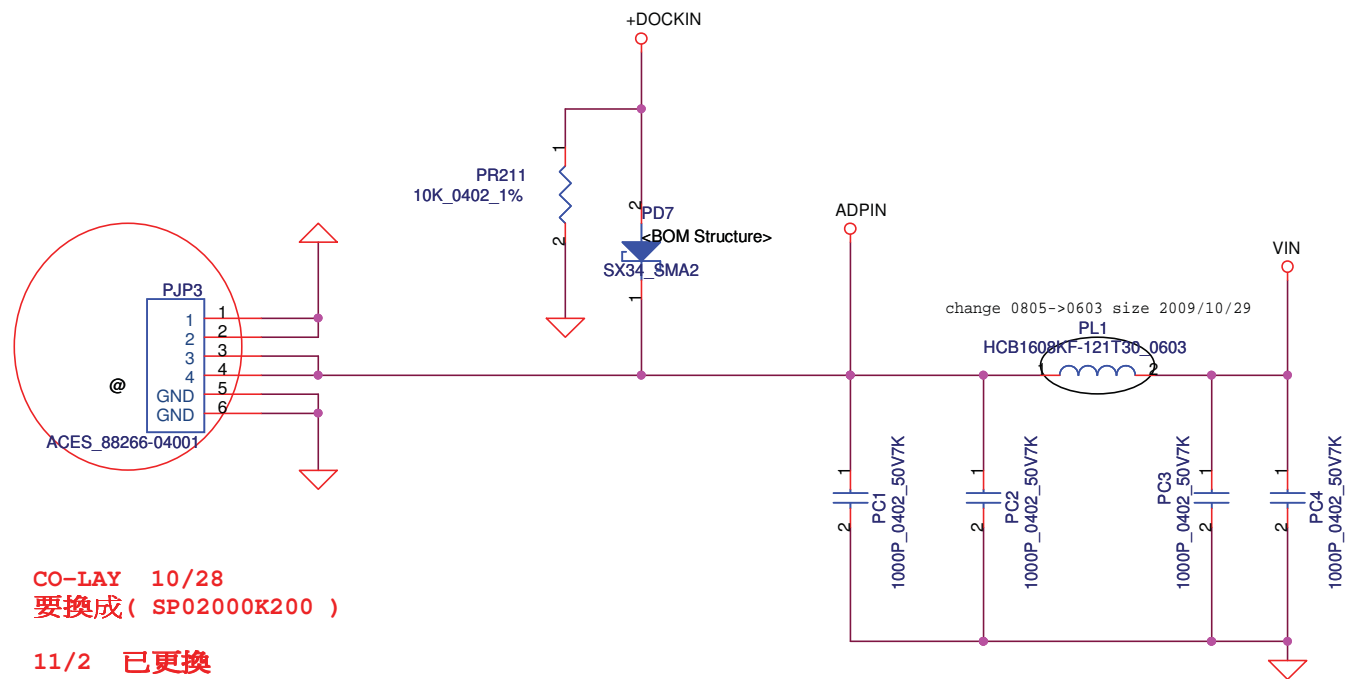


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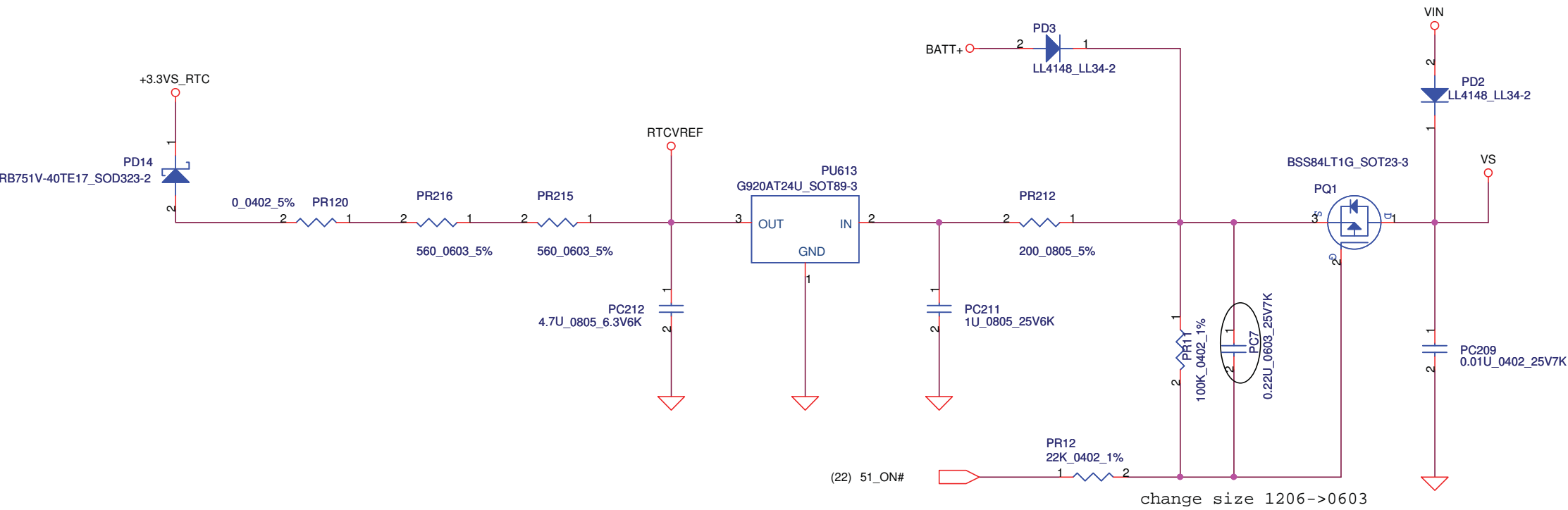


connect to PMU

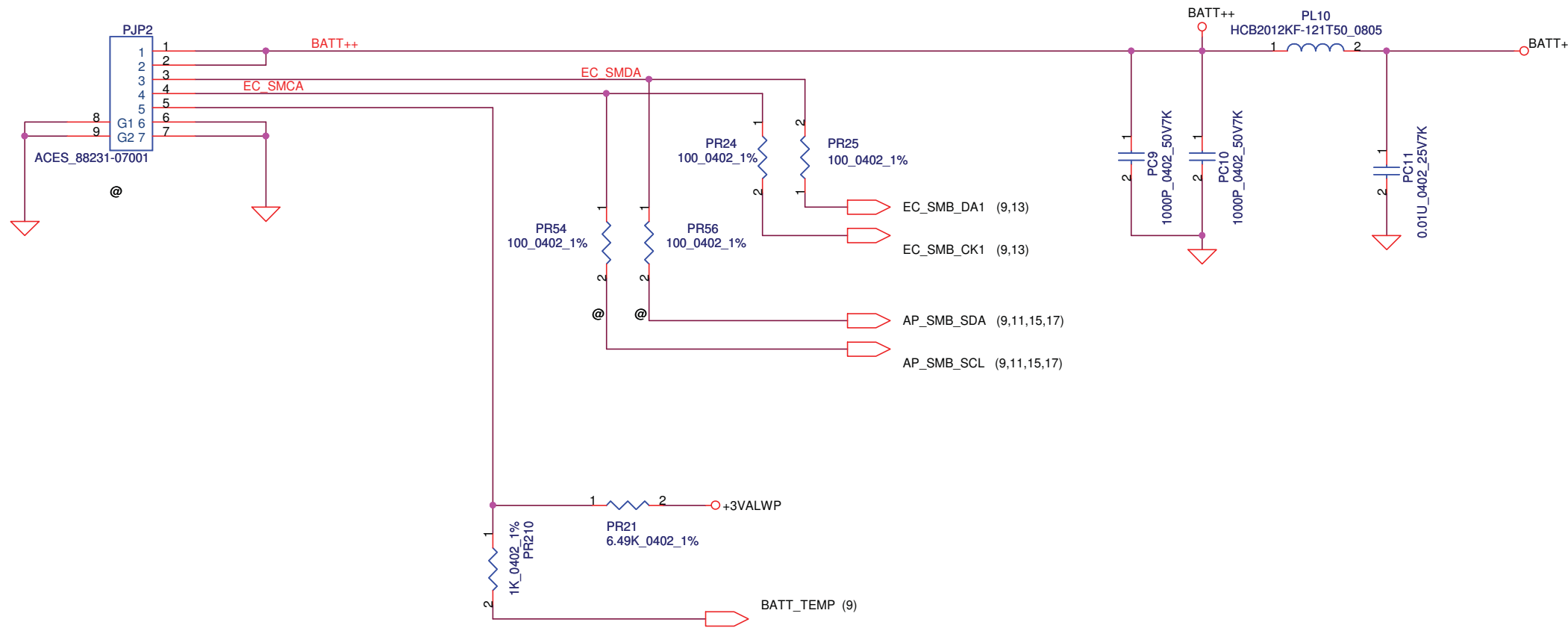
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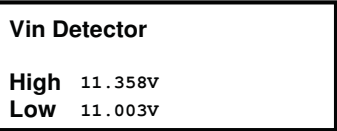
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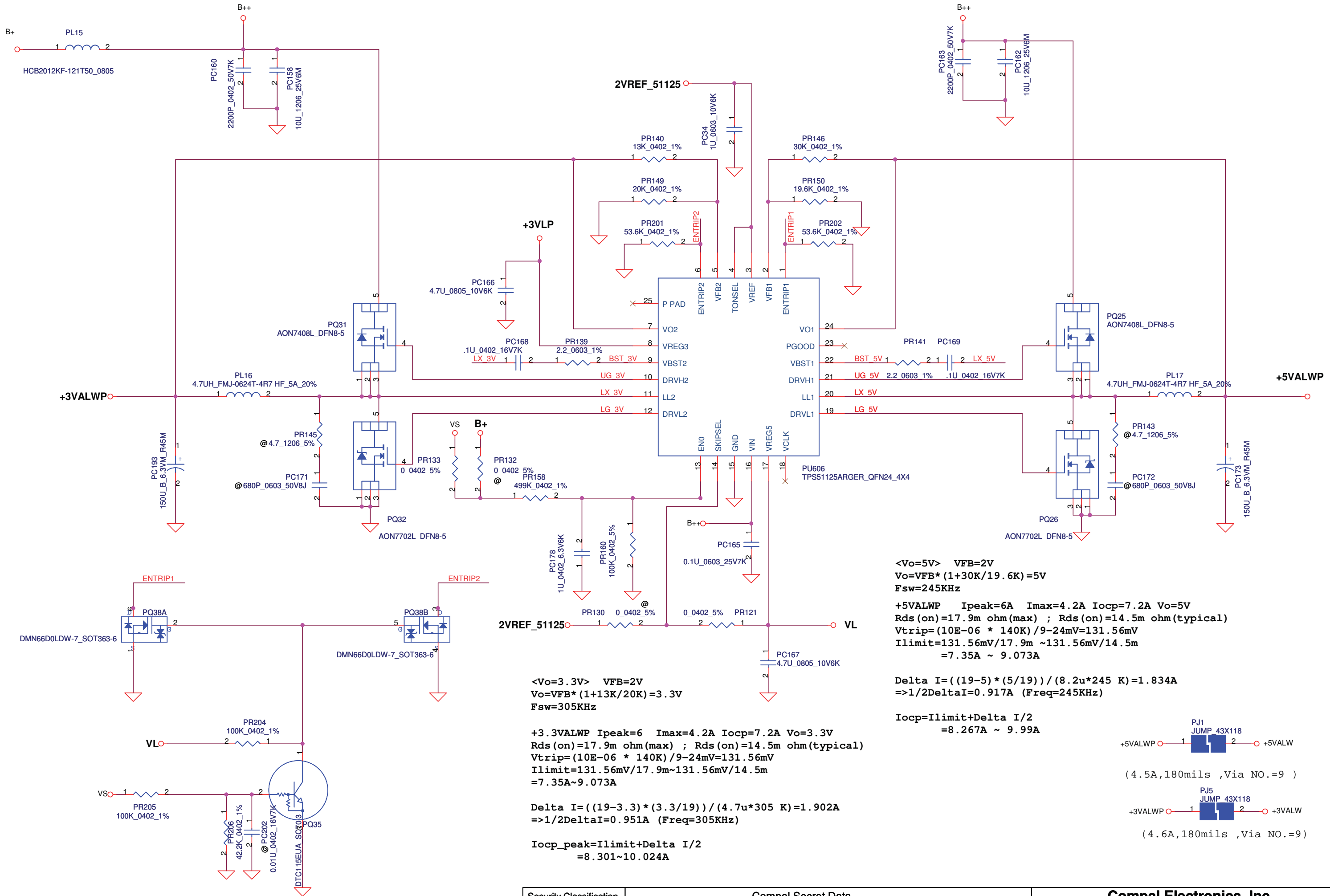
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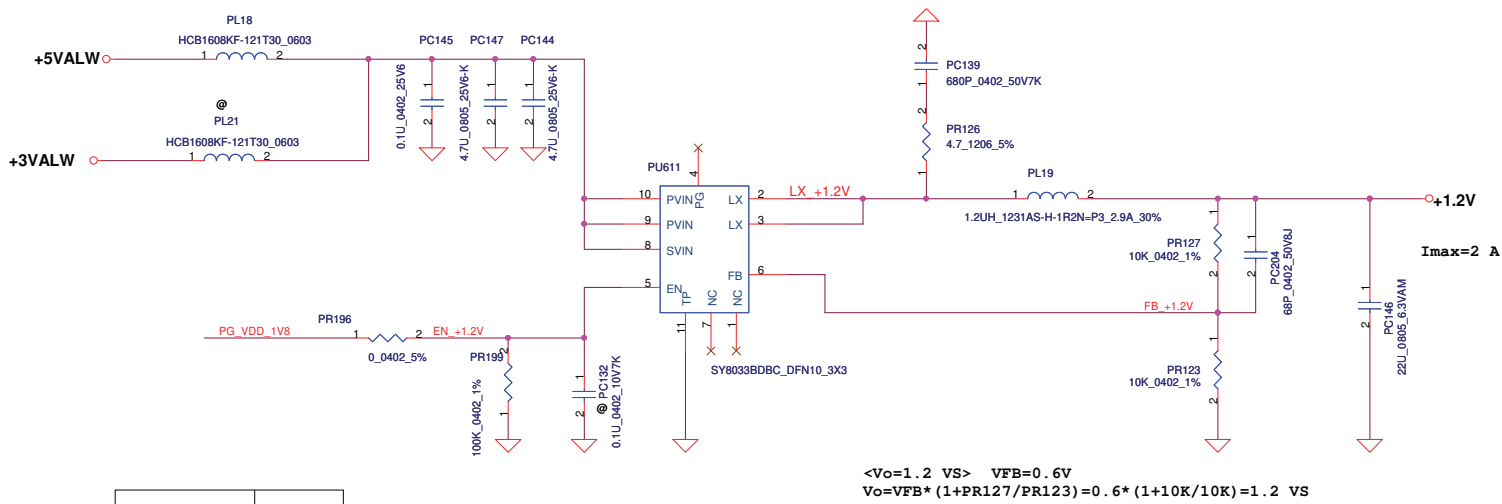
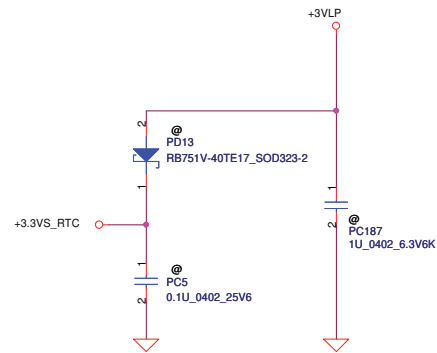
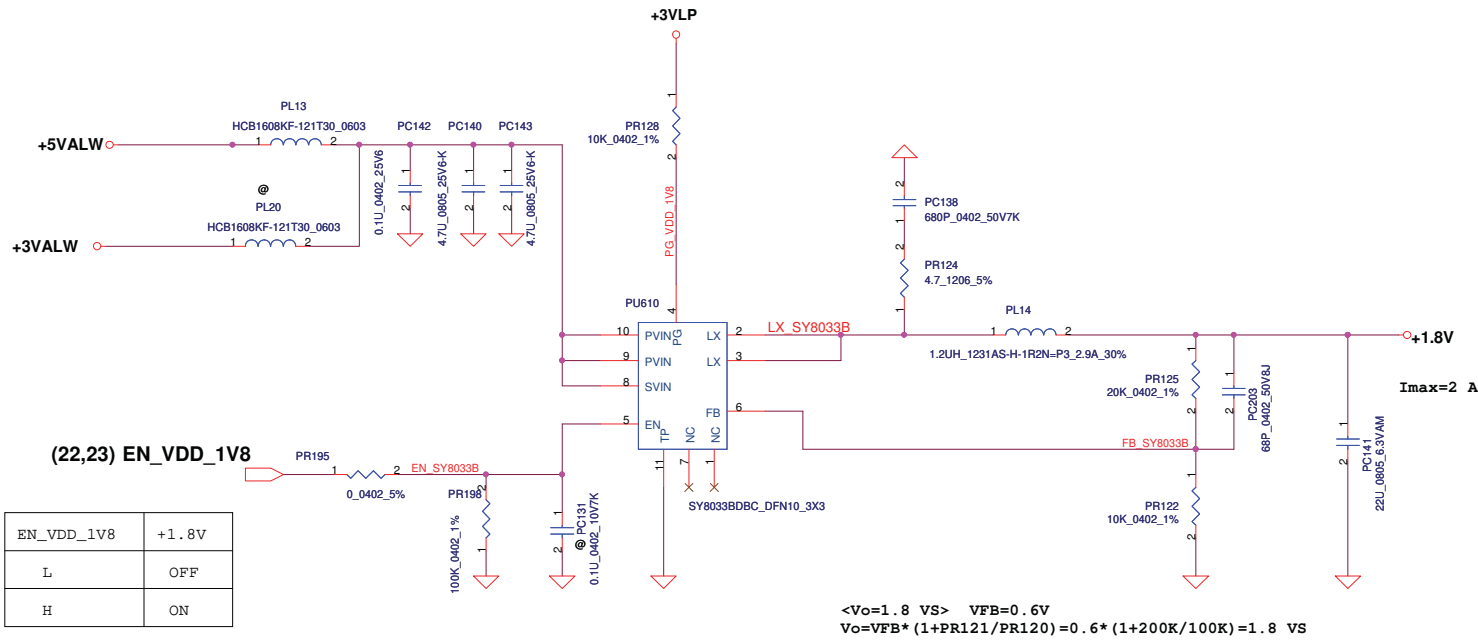
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					0.2
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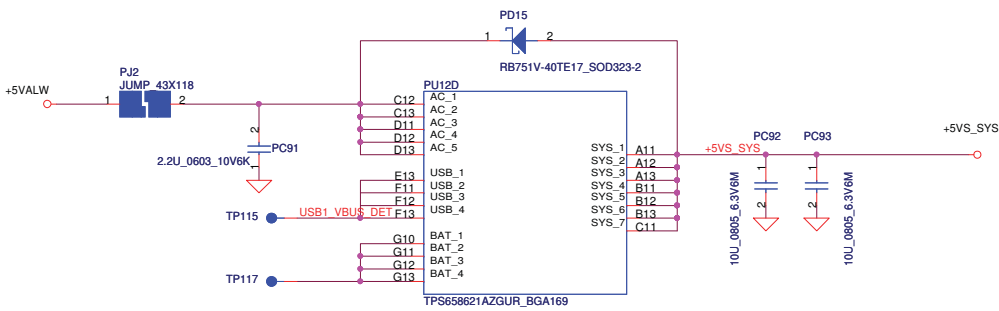
CHGVADJ	CV mode
0V	4V
1.885V	4.2V
3.3V	4.35V



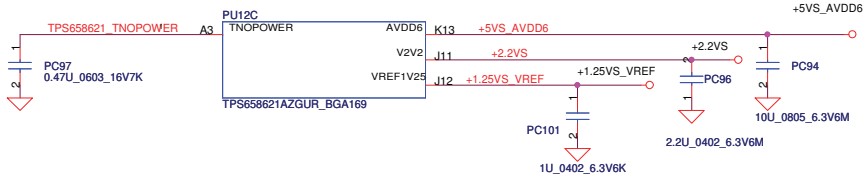
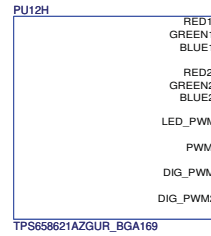
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				Size Custom	Document Number LA-6531P
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				+1.8VS		
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				Custom	LA-6531P	0.2
				Date:	Friday, December 24, 2010	Sheet 28 of 36



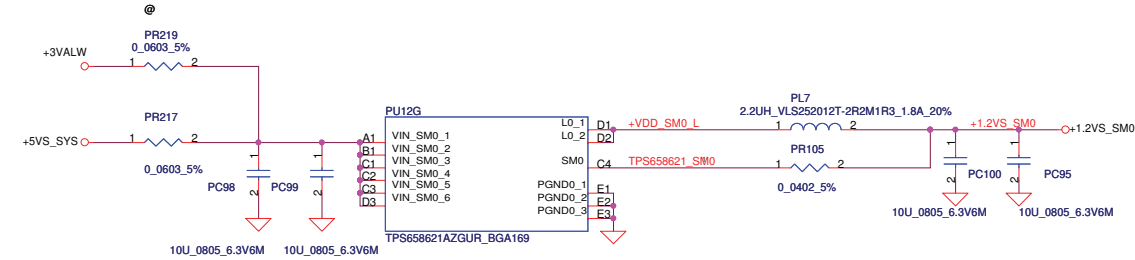
+VDD_SYS=5V
MAX current=1A



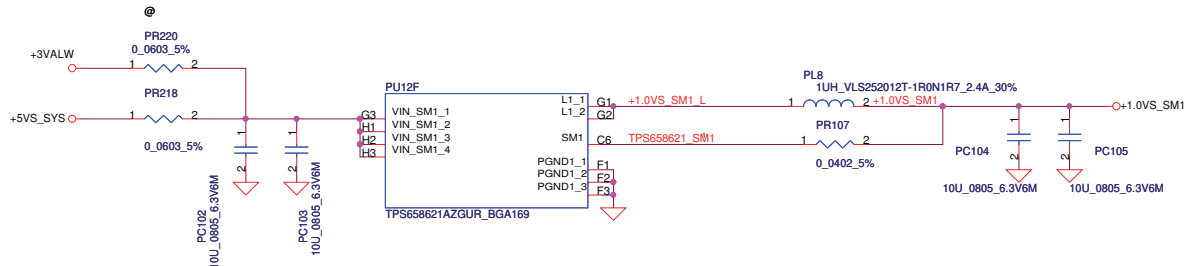
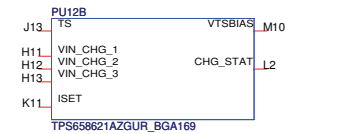
+VDD_AVDD6 =5V
MAX current=0.01A

+VDD_V2V2 =2.2V
MAX current=0.025A

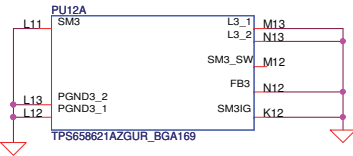
+VDD_VREF1V25 =1.25V
MAX current=0.01A



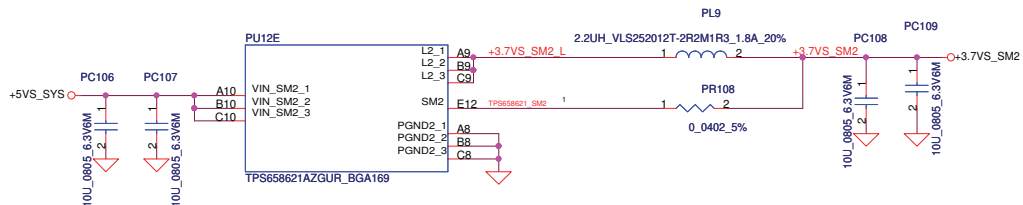
+VDD_SM0=1.2V
MAX current=0.6A



+VDD_SM1=1V
MAX current=1.5A



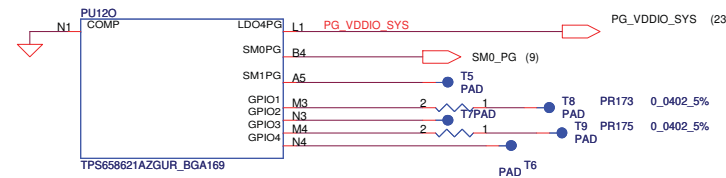
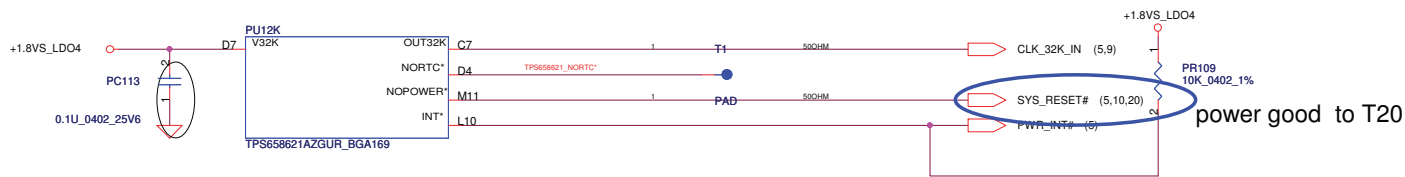
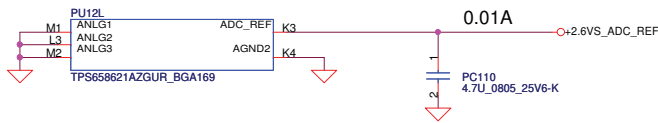
BOOST Converter



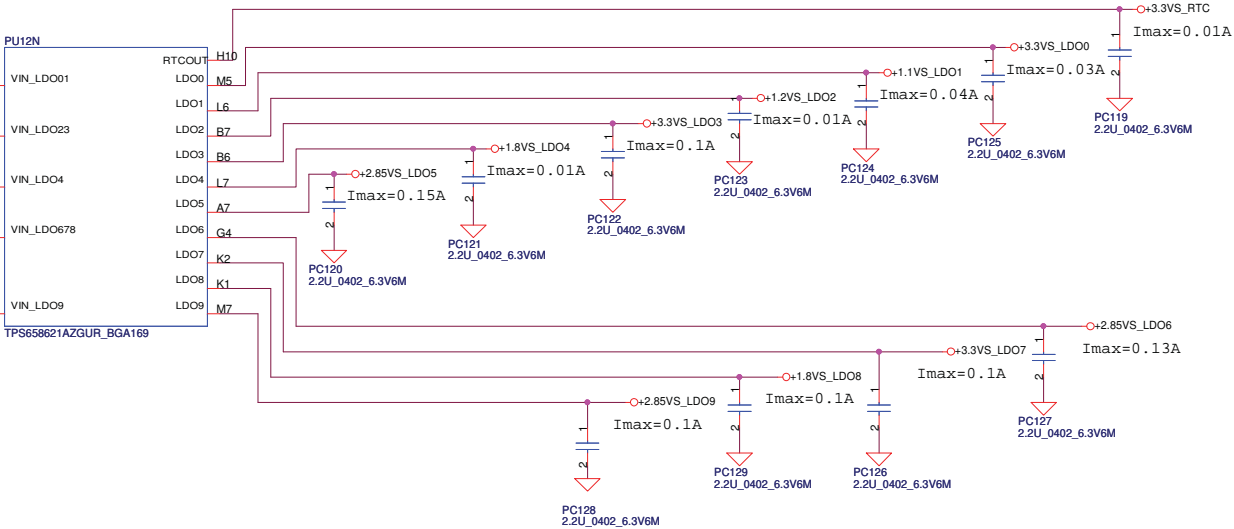
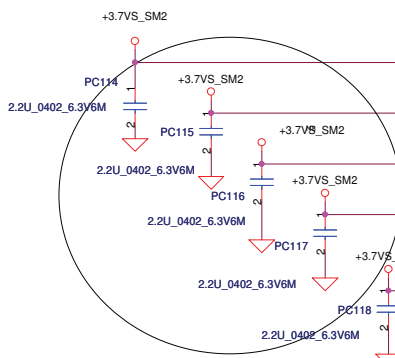
+VDD_SM2=3.7V
MAX current=0.75A

PMU #1

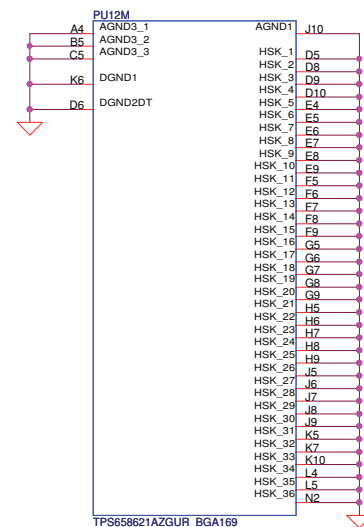
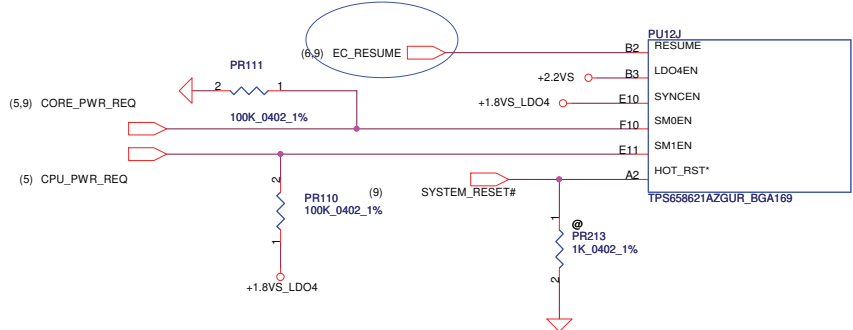
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2006/08/18		2008/09/20		PMU#1	
Size		Document Number		Rev	
Custom		LA-6531P		0.2	
Date:		Tuesday, December 21, 2010		Sheet 29 of 36	



LAYOUT元件擺IC出PIN

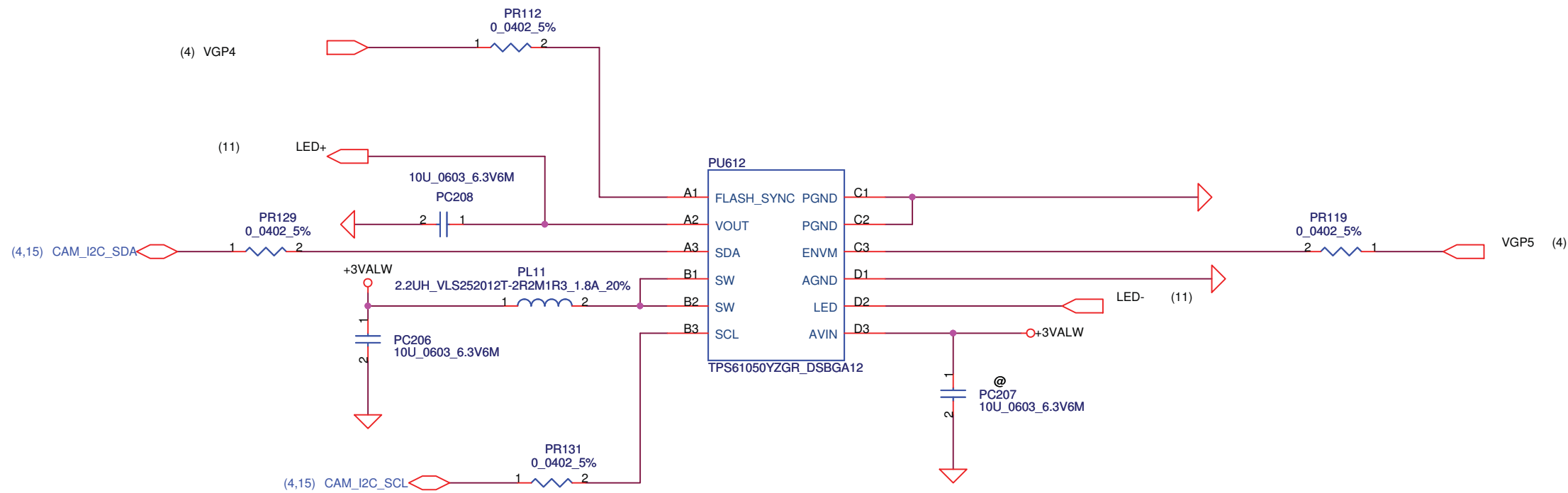


接到EC (POWER BUTTON)



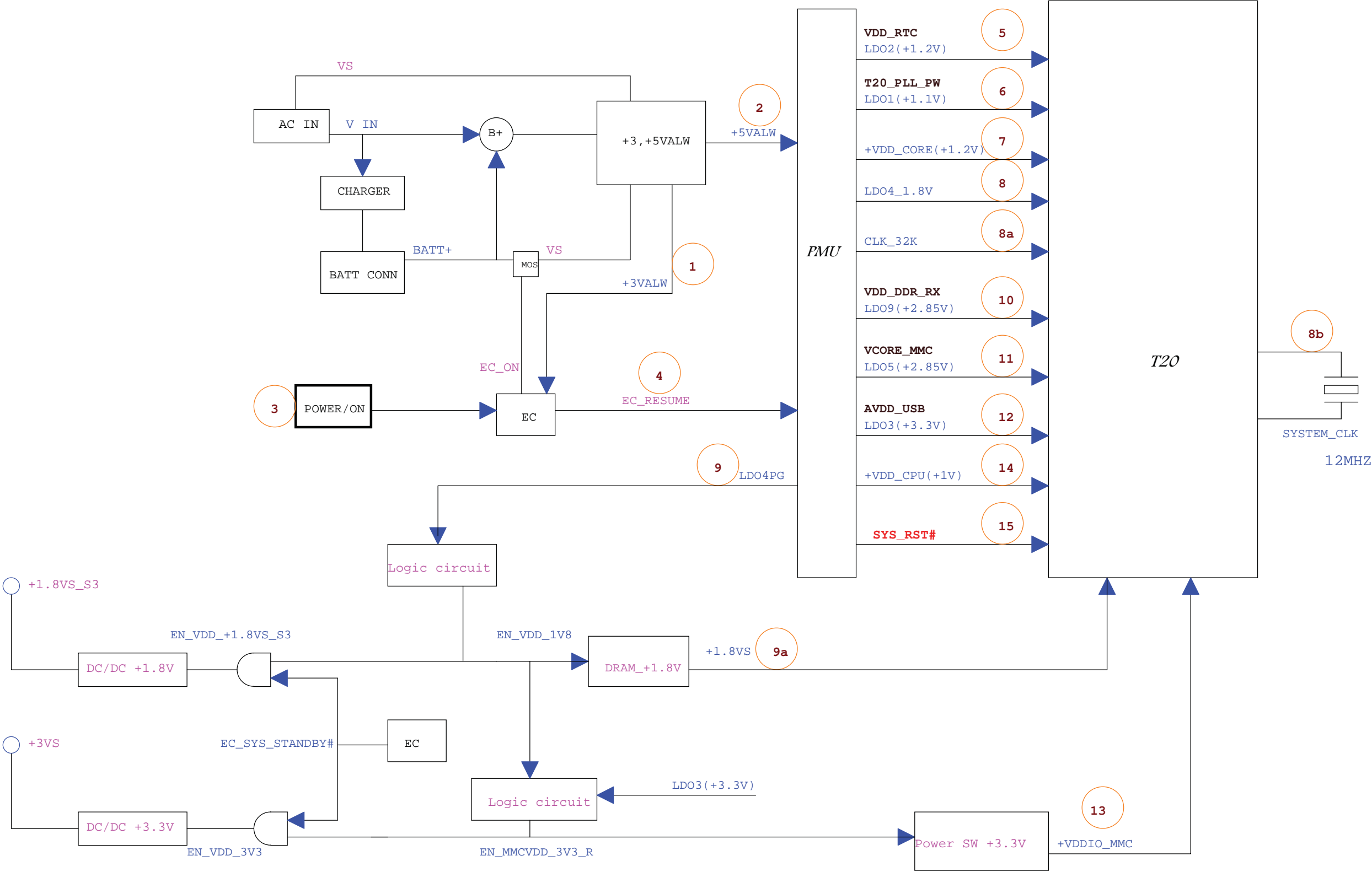
PMU #2

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				Custom	0.2
				Date:	Friday, December 24, 2010
				Sheet	30 of 36

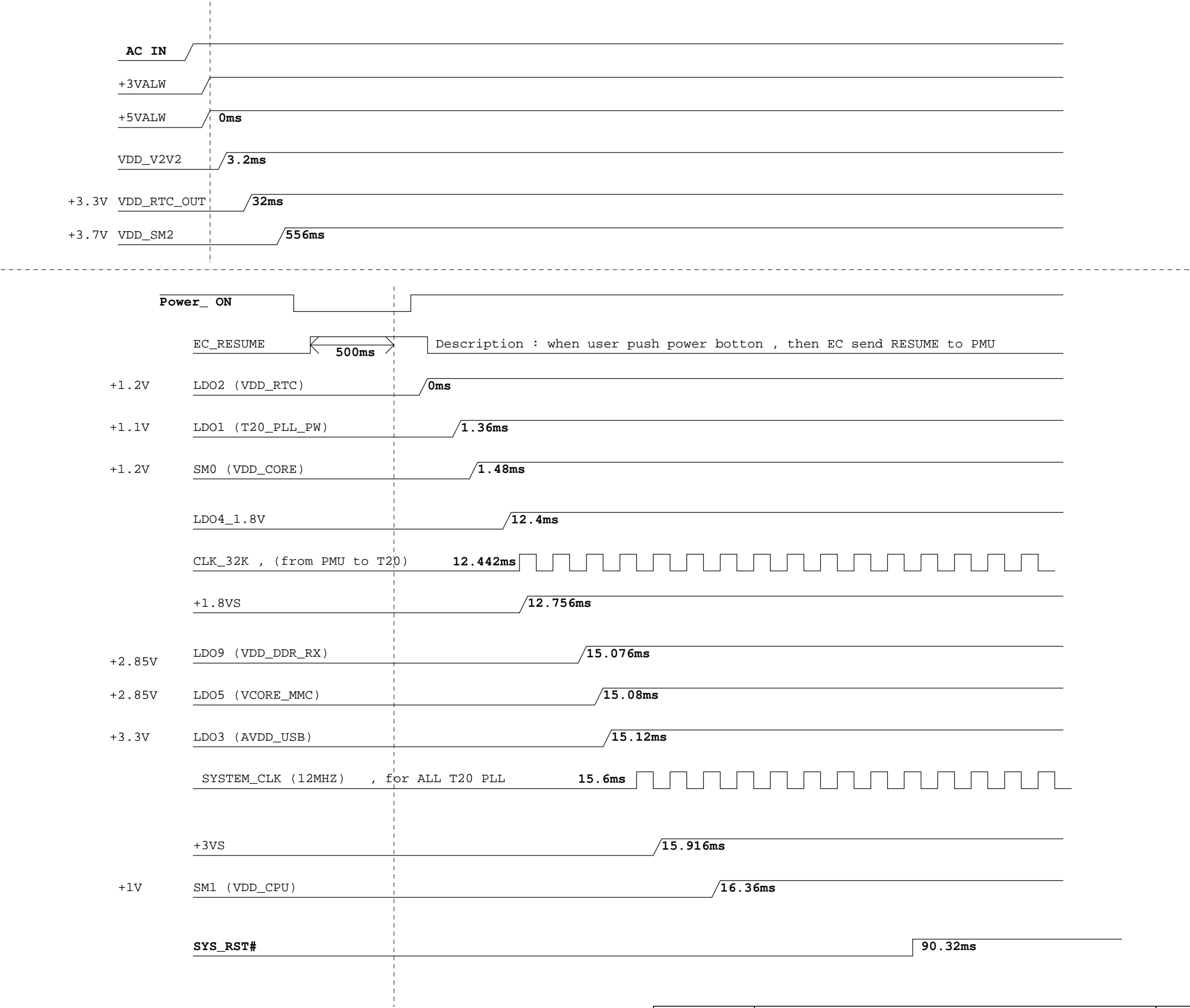


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				Size A3	Document Number LA-6531P	Rev 0.2
				Date:	Wednesday, January 05, 2011	Sheet 31 of 36

PBJ20 Power Sequence Flow Chart

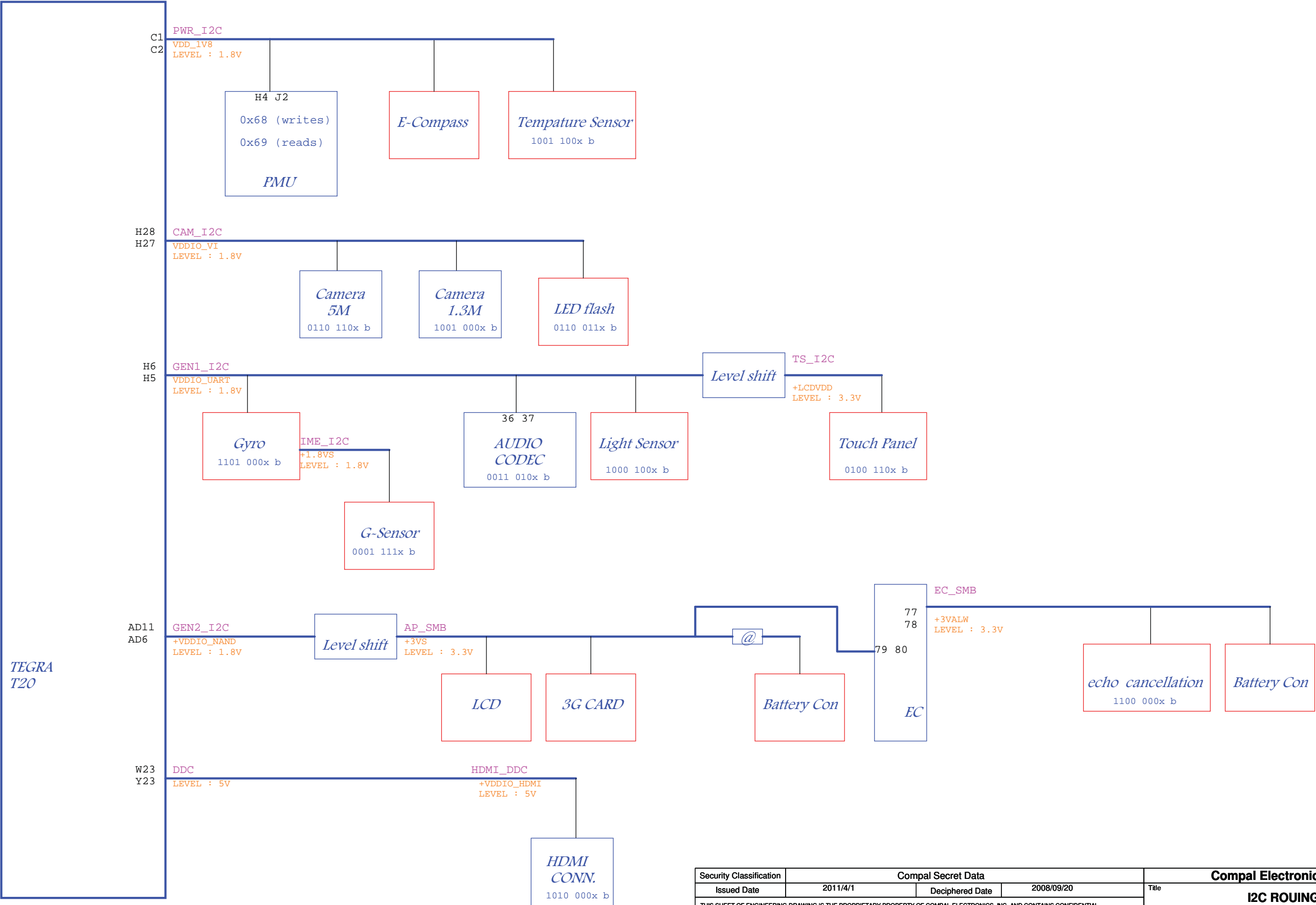


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				Size	Document Number	Rev
				Custom	LA-6531P	0.1
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				Size	Document Number	Rev
				Custom	LA-6531P	0.1
				Date:	Saturday, August 07, 2010	Sheet 33 of 36

PBJ20 I2C Routing



Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		增加控制CAMERA的GPIO	A		add CAM1_PWDN,CAM2_OE,CAM2_RST#,CAM1_RST#	08/29	DVT
2		修改EC firmware pin define	A		add KSI4,KSI5,KSI6,KSI7	08/29	DVT
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